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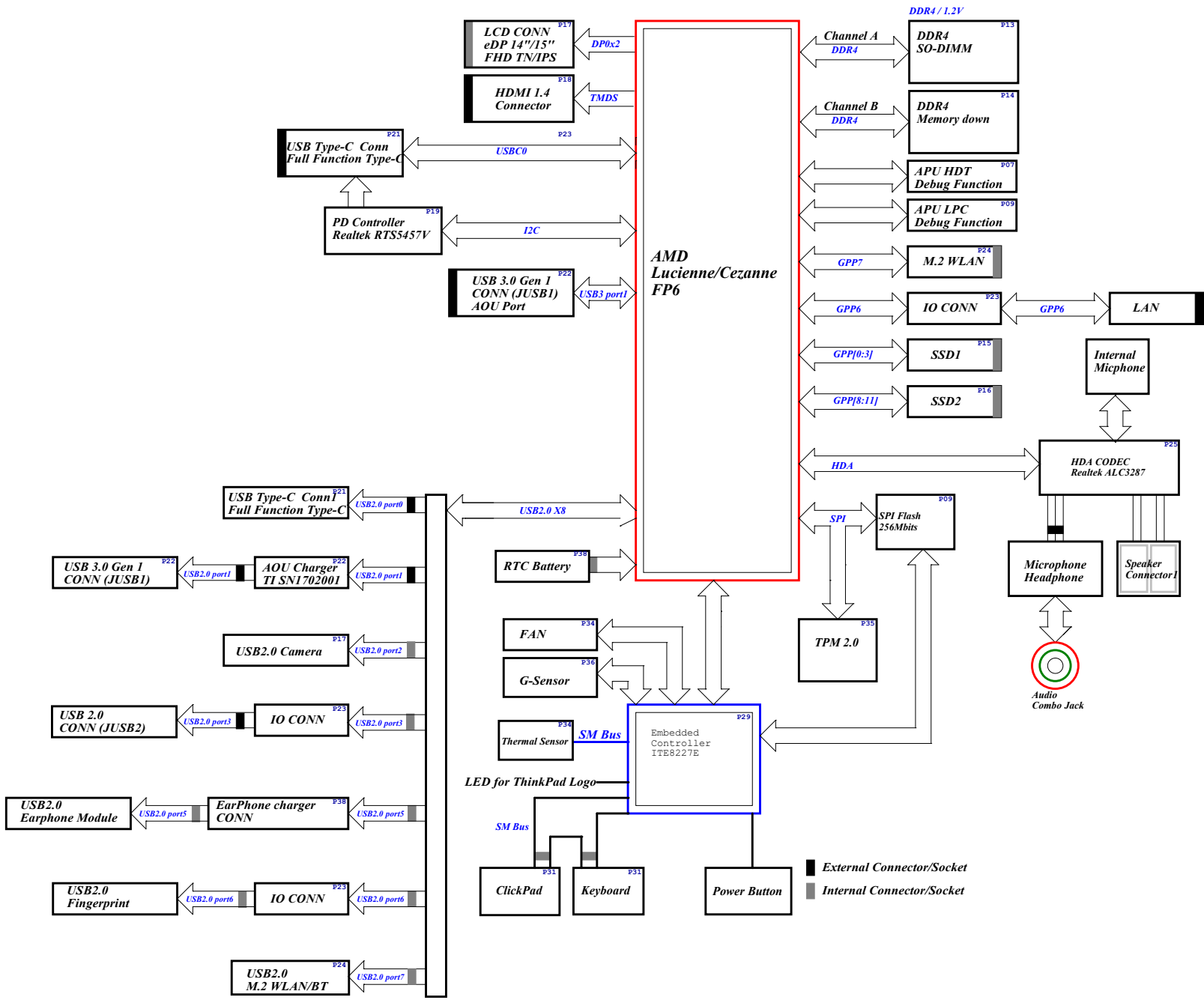
E14/E15 GEN3 Rev1.0 Schematic

*AMD Lucienne/Cezanne FP6 Processor with DDR4
NM-D481*

2021-01-23 Rev1.0

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2019/06/21	Deciphered Date	2019/06/21	COVER PAGE	
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STATE	SIGNAL	SLP_S3#	SUSP#	SLP_S5#	SYSON	EC_ON	
S0		HIGH		HIGH		ON	
S3 (Suspend to RAM)		LOW		HIGH		ON	
S4 (Suspend to Disk)		LOW		LOW		ON	
S5 (Soft OFF)		LOW		LOW		ON	

USB2 Port

Port	Device
0	USBC Type-C
1	USB3.0 port
2	Camera
3	USB2.0 Port
4	X
5	Earphone charge
6	FingerPrint
7	BT

USB3 Port

Port	Device
0	USBC Type-C
1	USB3.0 port
4	X
5	X

PCIe Port

Port	Device
GPP0~3	SSD1
GPP4	X
GPP5	X
GPP6	LAN
GPP7	WLAN
GPP8~11	SSD2
GFX0~7	X

Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane	B9+	+3VALW	+1.2V	+5VS
State		+5VALW	+2.5V	+3VS
		+1.8VALW		+1.8VS
		+0.75VALW_VDDP		+0.75VS_VDDP
				+0.6VS
				+VDDCR_SOC
				+VDDC_VDD
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
G3 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

EC	Schemic	SOURCE	PMIC	BATT	Charge	PD	APU	USB3.1 Redriver	G-Sensor	Thermal Sensor	SODIMM	CP Module
SMCLK0 SMDAT0	EC_SMB_CK0 EC_SMB_DA0	EC +3VL	V +3VL	X	X	X	V +3VS	X	X	X	X	X
SMCLK1 SMDAT1	EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V +3VL	V +3VL	X	X	X	X	X	X	X
SMCLK2 SMDAT2	EC_SMB_CK2 EC_SMB_DA2	EC +3VL	X	X	X	V +3VL	X	X	X	X	X	X
SMCLK3 SMDAT3	EC_SMB_CK3 EC_SMB_DA3	EC +3VS	X	X	X	X	X	X	X	X	X	X
SMCLK4 SMDAT4	EC_SMB_CK4 EC_SMB_DA4	EC +3VS	X	X	X	X	X	X	V +3VS	V +3VS	X	X
	APU_SMB0CLK APU_SMB0DATA	APU +3VS	X	X	X	X	X	X	X	X	V +3VS	X
	APU_SMB1CLK APU_SMB1DATA	APU +3VALW	X	X	X	X	X	X	X	X	X	V +3VS

PD Controller I2C

	SOURCE	APU
I2C_M_SCL I2C_M_SDA	PD +LDO_3V3	V +1.8VALW

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BOM Structure Table

BOM Structure	NOTE
HDT#	For HDT AMD debug port
LPC#	For LPC AMD debug port
RCM#	SPI RCM
PD_AOU#	Type A AOU function by PDC
TPM#	Trusted Platform Module (TPM)
HDMI#	HDMI LOGO
CD#	COST DOWN
ME#	ME Connector
EMC#	For EMI function
EMC_NS#	EMC Reserves
RF#	For RF function
RF_NS#	RF Reserves
FP#	Finger printer
AOU#	AOU charger for Type A
AOAC#	For WLAN AOAC
EAR#	Bluetooth earphone
EMC_EAR#	EMC For Bluetooth earphone

M.2 SSD1

15 PCIE0_SSD_RX_P
15 PCIE0_SSD_RX_N
15 PCIE1_SSD_RX_P
15 PCIE1_SSD_RX_N
15 PCIE2_SSD_RX_P
15 PCIE2_SSD_RX_N
15 PCIE3_SSD_RX_P
15 PCIE3_SSD_RX_N

PCIE0_SSD_RX_P
PCIE0_SSD_RX_N
PCIE1_SSD_RX_P
PCIE1_SSD_RX_N
PCIE2_SSD_RX_P
PCIE2_SSD_RX_N
PCIE3_SSD_RX_P
PCIE3_SSD_RX_N

G11 P_GPP_RXP0
F11 P_GPP_RXN0
J10 P_GPP_RXP1
H10 P_GPP_RXN1
G8 P_GPP_RXP2/SATA0_RXP
F8 P_GPP_RXN2/SATA0_RXN
G6 P_GPP_RXP3/SATA1_RXP
F7 P_GPP_RXN3/SATA1_RXN

L3 PCIE0_TX_P
L1 PCIE0_TX_N
L4 PCIE1_TX_P
L2 PCIE1_TX_N
M4 PCIE2_TX_P
M2 PCIE2_TX_N
N3 PCIE3_TX_P
N1 PCIE3_TX_N

CC1 1 2 0.22U 6.3V K XSR 0201
CC2 1 2 0.22U 6.3V K XSR 0201
CC3 1 2 0.22U 6.3V K XSR 0201
CC4 1 2 0.22U 6.3V K XSR 0201
CC5 1 2 0.22U 6.3V K XSR 0201
CC6 1 2 0.22U 6.3V K XSR 0201
CC7 1 2 0.22U 6.3V K XSR 0201
CC8 1 2 0.22U 6.3V K XSR 0201

PCIE0_SSD_TX_P
PCIE0_SSD_TX_N
PCIE1_SSD_TX_P
PCIE1_SSD_TX_N
PCIE2_SSD_TX_P
PCIE2_SSD_TX_N
PCIE3_SSD_TX_P
PCIE3_SSD_TX_N

15 PCIE0_SSD_TX_P
15 PCIE0_SSD_TX_N
15 PCIE1_SSD_TX_P
15 PCIE1_SSD_TX_N
15 PCIE2_SSD_TX_P
15 PCIE2_SSD_TX_N
15 PCIE3_SSD_TX_P
15 PCIE3_SSD_TX_N

M.2 SSD1

LAN

WLAN

23 PCIE6_LAN_RX_P
23 PCIE6_LAN_RX_N
24 PCIE7_WLAN_RX_P
24 PCIE7_WLAN_RX_N

PCIE6_LAN_RX_P
PCIE6_LAN_RX_N
PCIE7_WLAN_RX_P
PCIE7_WLAN_RX_N

K7 P_GPP_RXP6
K8 P_GPP_RXN6
H6 P_GPP_RXP7
H7 P_GPP_RXN7

P_GPP_TXP6
P_GPP_TXN6
P_GPP_TXP7
P_GPP_TXN7

CC9 1 2 0.1U 6.3V K XSR 0201
CC10 1 2 0.1U 6.3V K XSR 0201
CC11 1 2 0.1U 6.3V K XSR 0201
CC12 1 2 0.1U 6.3V K XSR 0201

PCIE6_LAN_TX_P
PCIE6_LAN_TX_N
PCIE7_WLAN_TX_P
PCIE7_WLAN_TX_N

23 PCIE6_LAN_TX_P
23 PCIE6_LAN_TX_N
24 PCIE7_WLAN_TX_P
24 PCIE7_WLAN_TX_N

LAN

WLAN

M.2 SSD2

16 PCIE8_SSD_RX_P
16 PCIE8_SSD_RX_N
16 PCIE9_SSD_RX_P
16 PCIE9_SSD_RX_N
16 PCIE10_SSD_RX_P
16 PCIE10_SSD_RX_N
16 PCIE11_SSD_RX_P
16 PCIE11_SSD_RX_N

PCIE8_SSD_RX_P
PCIE8_SSD_RX_N
PCIE9_SSD_RX_P
PCIE9_SSD_RX_N
PCIE10_SSD_RX_P
PCIE10_SSD_RX_N
PCIE11_SSD_RX_P
PCIE11_SSD_RX_N

L9 P_GPP_RXP8/SATA2_RXP
L10 P_GPP_RXN8/SATA2_RXN
K11 P_GPP_RXP9/SATA3_RXP
J11 P_GPP_RXN9/SATA3_RXN
J12 P_GPP_RXP10
H12 P_GPP_RXN10
J13 P_GPP_RXP11
K13 P_GPP_RXN11

P_GPP_TXP8/SATA2_TXP
P_GPP_TXN8/SATA2_TXN
P_GPP_TXP9/SATA3_TXP
P_GPP_TXN9/SATA3_TXN
P_GPP_TXP10
P_GPP_TXN10
P_GPP_TXP11
P_GPP_TXN11

CC13 1 2 0.22U 6.3V K XSR 0201
CC14 1 2 0.22U 6.3V K XSR 0201
CC15 1 2 0.22U 6.3V K XSR 0201
CC16 1 2 0.22U 6.3V K XSR 0201
CC17 1 2 0.22U 6.3V K XSR 0201
CC18 1 2 0.22U 6.3V K XSR 0201
CC19 1 2 0.22U 6.3V K XSR 0201
CC20 1 2 0.22U 6.3V K XSR 0201

PCIE8_SSD_TX_P
PCIE8_SSD_TX_N
PCIE9_SSD_TX_P
PCIE9_SSD_TX_N
PCIE10_SSD_TX_P
PCIE10_SSD_TX_N
PCIE11_SSD_TX_P
PCIE11_SSD_TX_N

16 PCIE8_SSD_TX_P
16 PCIE8_SSD_TX_N
16 PCIE9_SSD_TX_P
16 PCIE9_SSD_TX_N
16 PCIE10_SSD_TX_P
16 PCIE10_SSD_TX_N
16 PCIE11_SSD_TX_P
16 PCIE11_SSD_TX_N

M.2 SSD2

FP6 REV0.32
PART 2/13

AMD-RENOIR-FP6_BGA1140

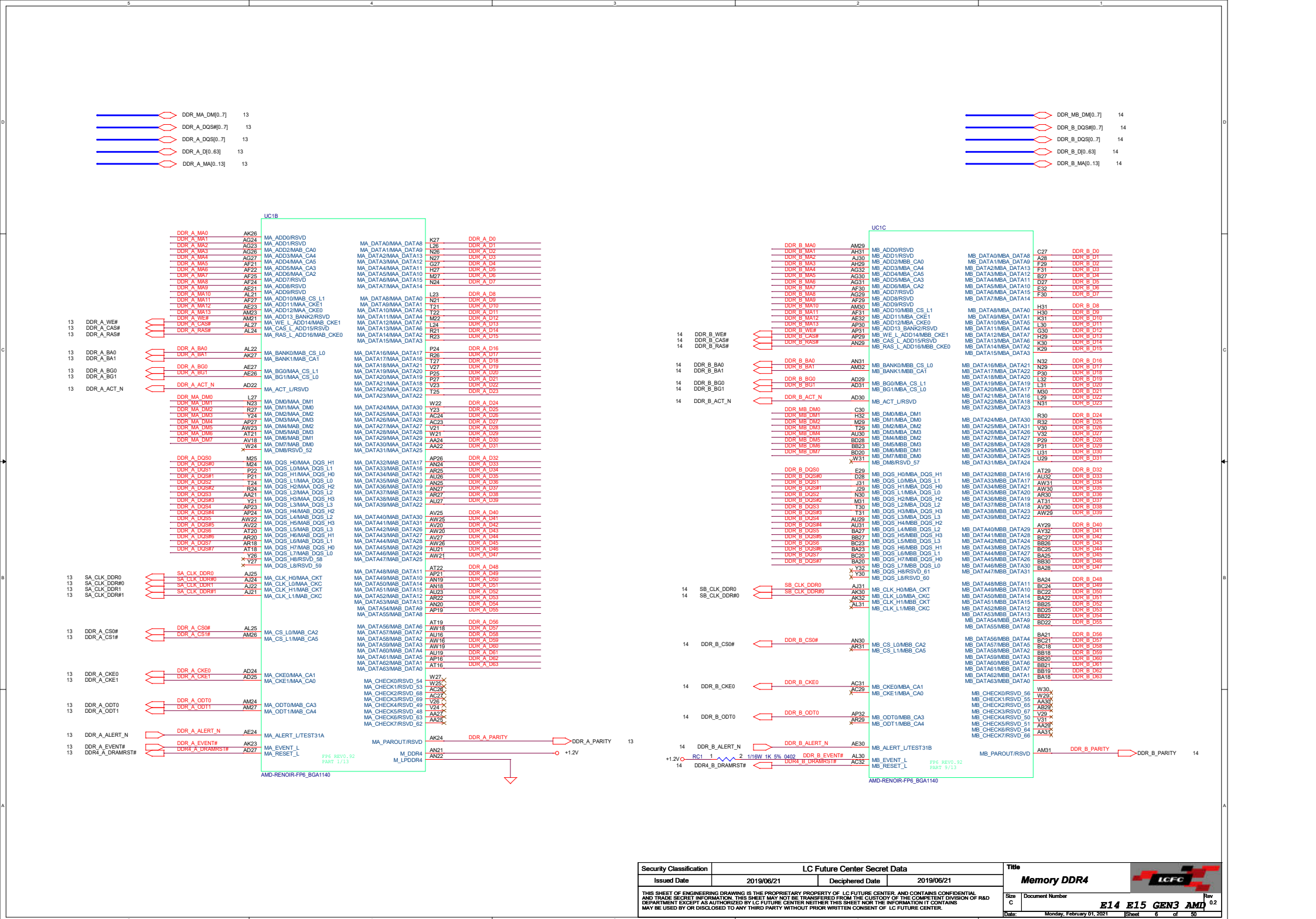
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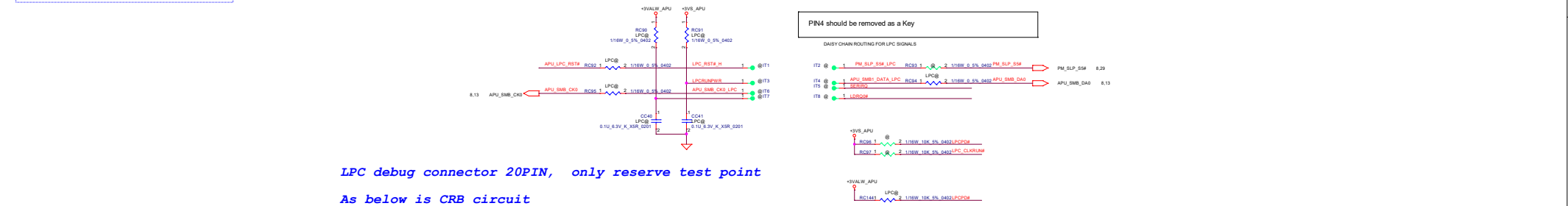
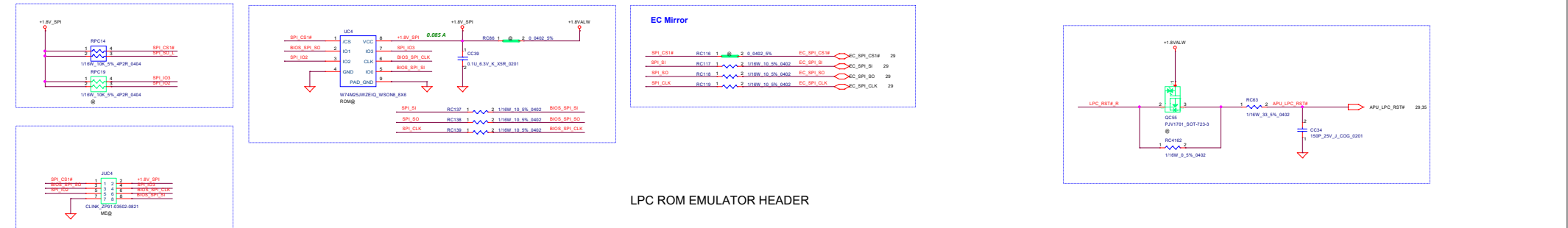
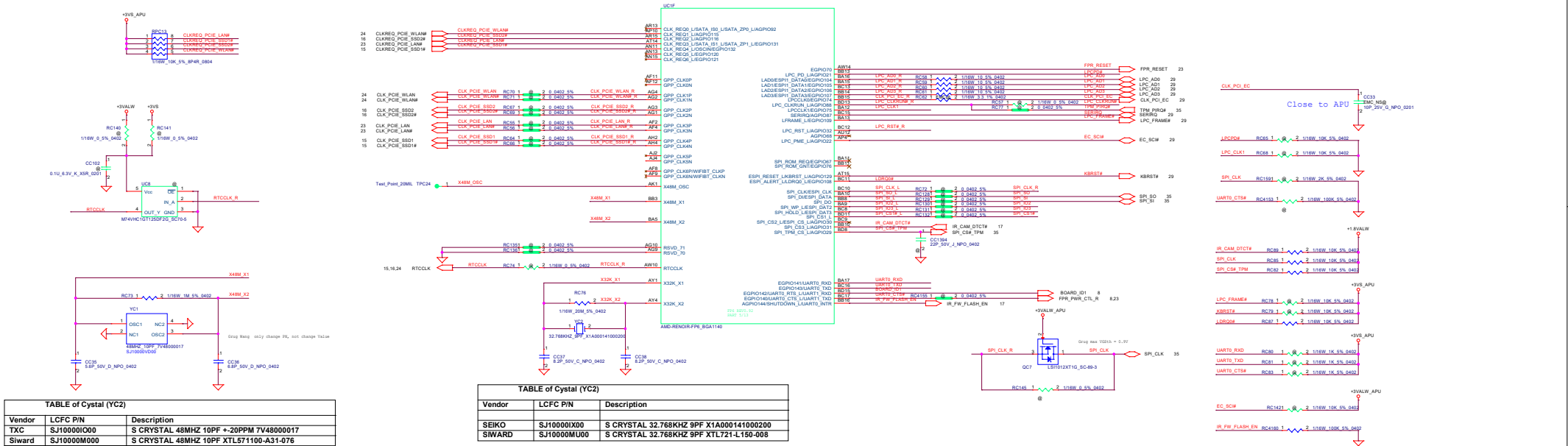
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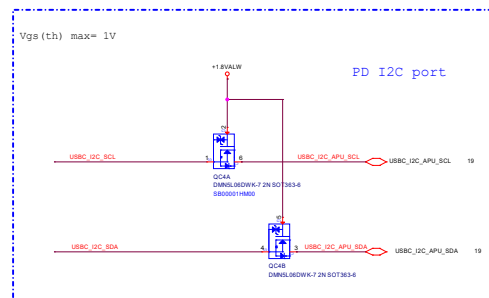
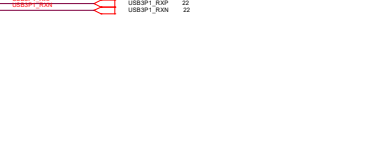
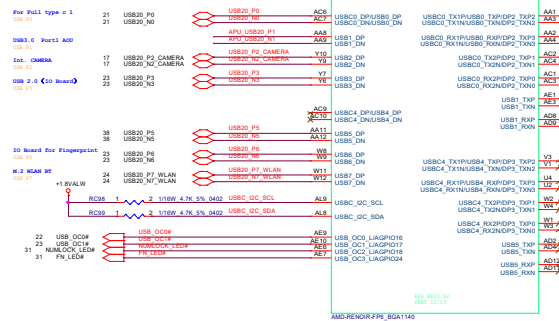
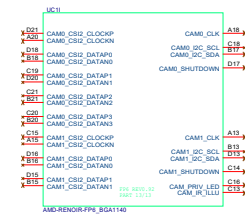
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Size C	Document Number	E14 E15 GEN3 AMD	
Date	Monday, February 01, 2021	Sheet	5 of 50




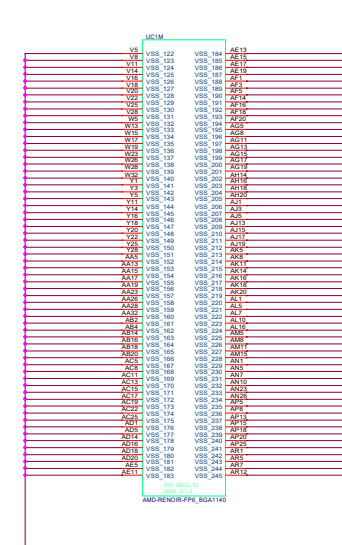
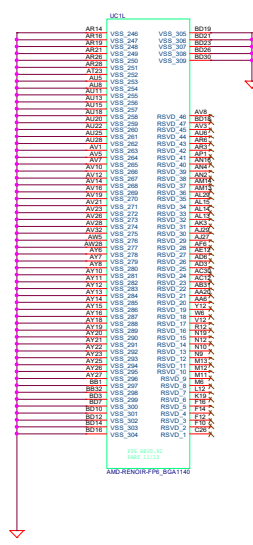
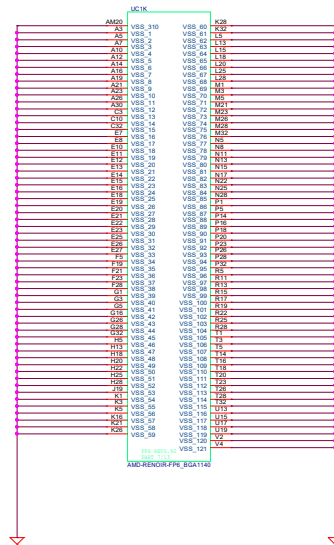
Rev 0.2



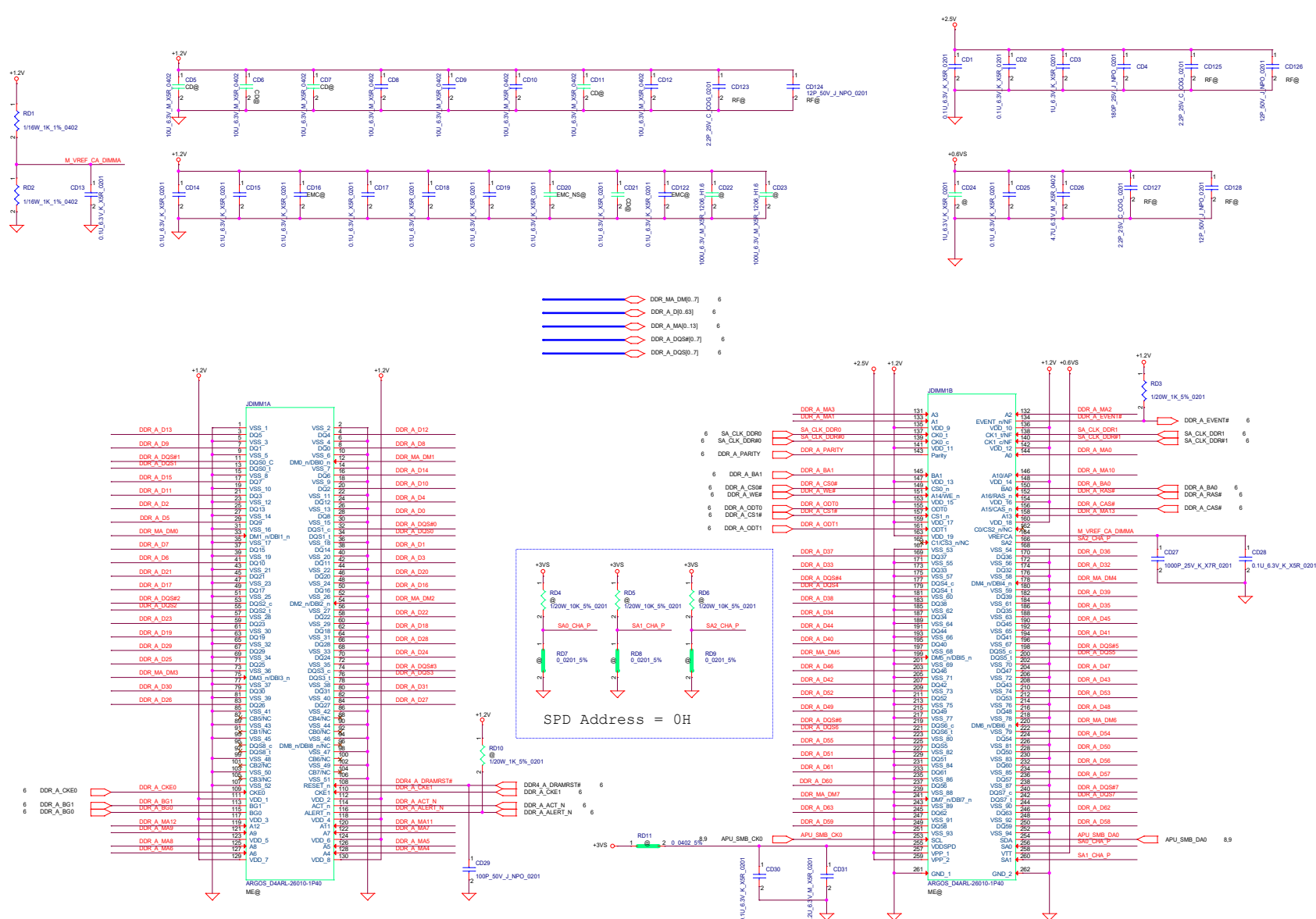




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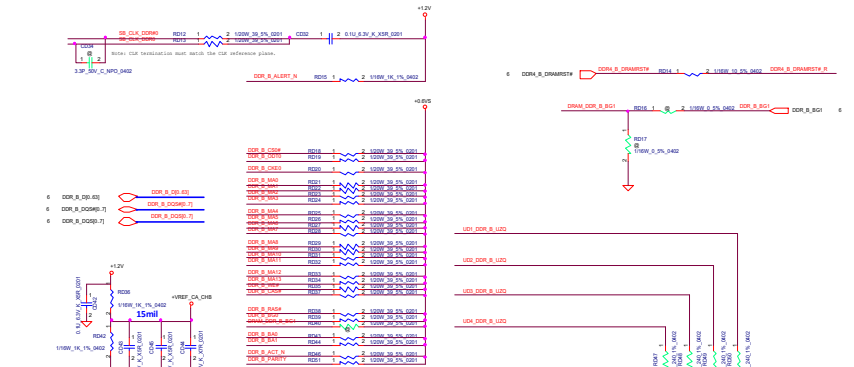
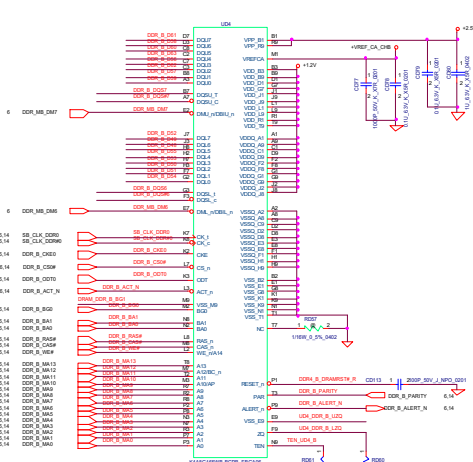
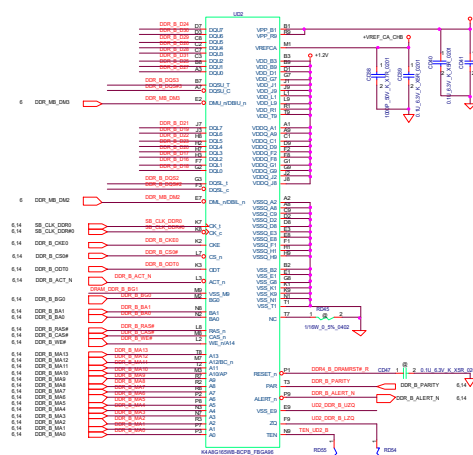
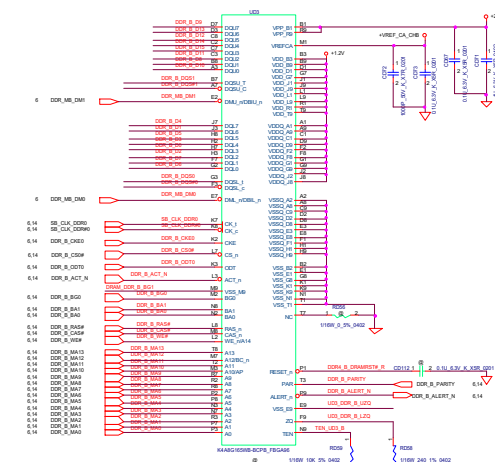
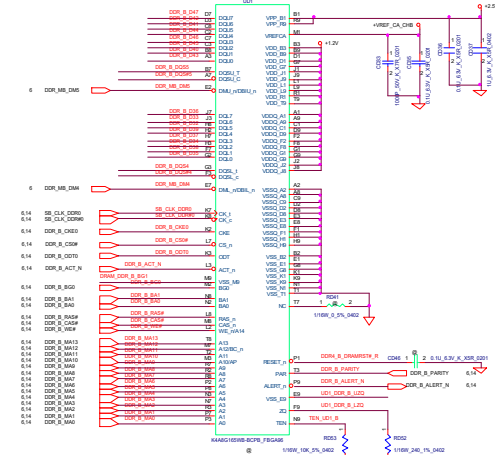


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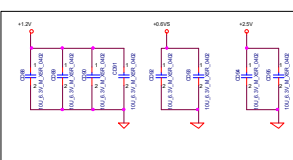
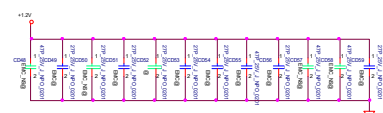


8Gb SDP
16Gb DDP

8Gb SDP
16Gb DDP

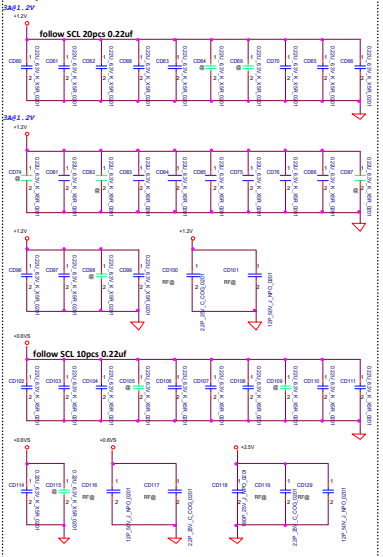


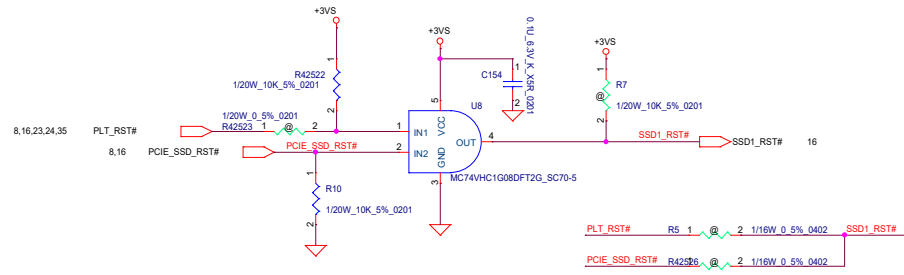
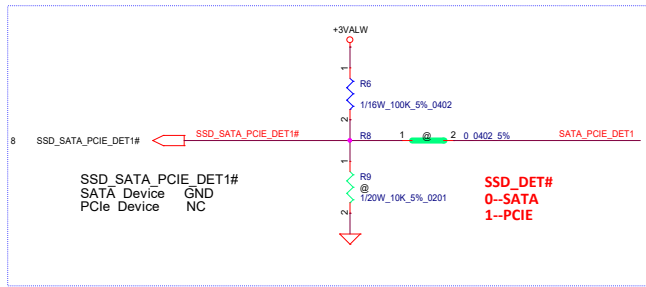
RD47 RD48 RD49 RD50 will install different value base on SDP or DDP control by Virtual symbol



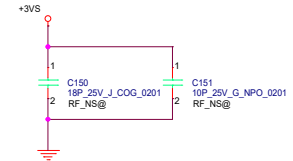
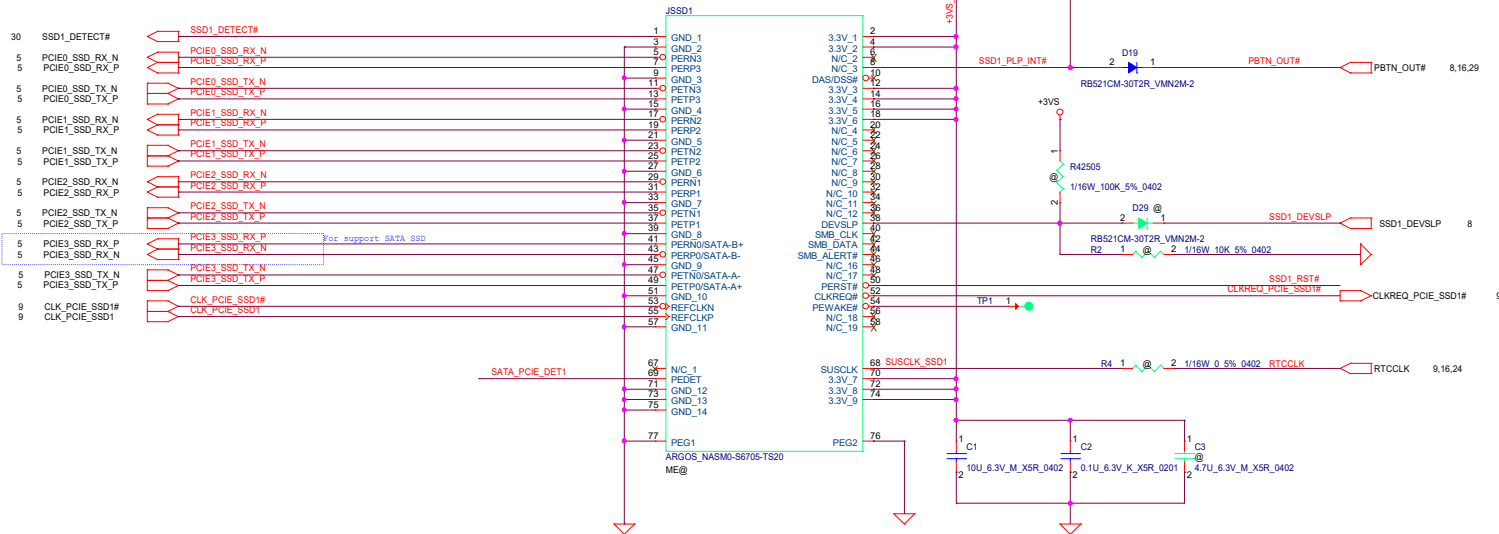
Capacitor Value	Configuration	VDDIO_MEN_S3-VSS	VDDIO_MEN_S3-VTT	VTT-VSS	VREF CA-VDDIO_MEN_S3
0.1uF	0402 XSR	SRx16	-	-	4
0.22uF	0402 XSR	SRx16	18	5	-

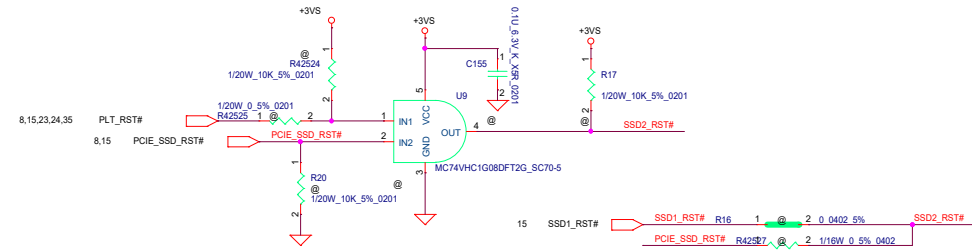
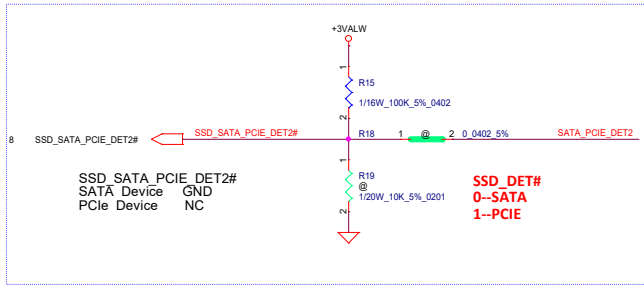
Layout Note: Place near DRAM



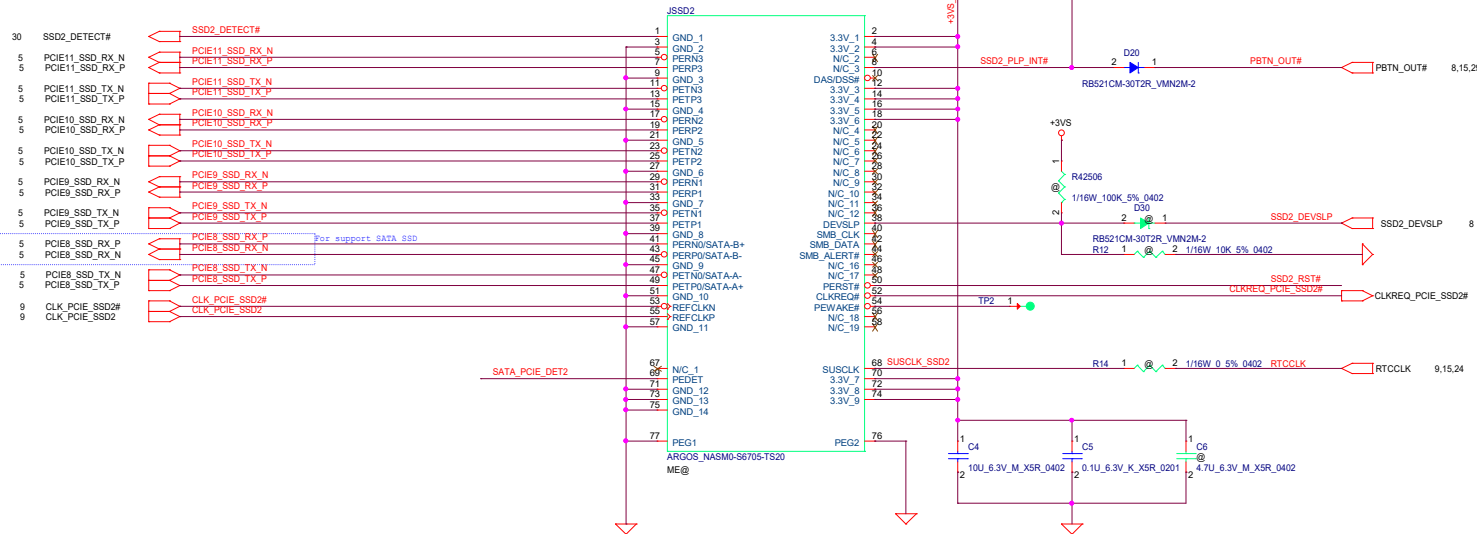


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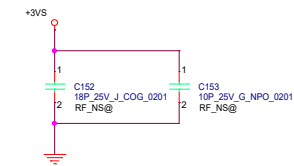


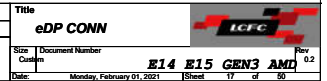
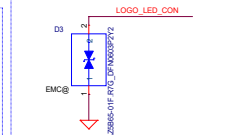
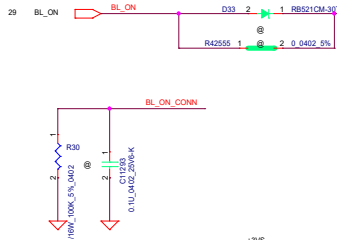
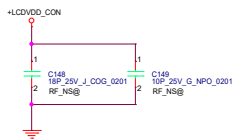
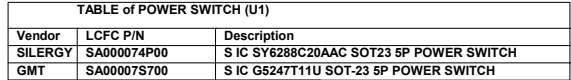


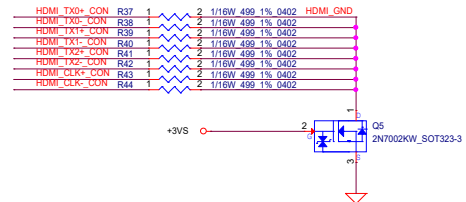
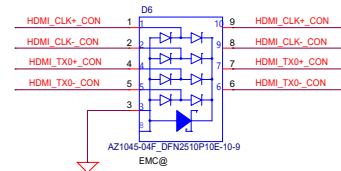
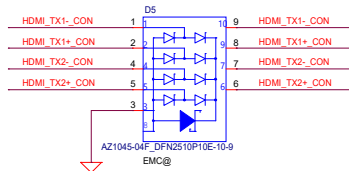
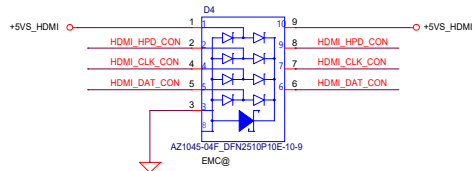
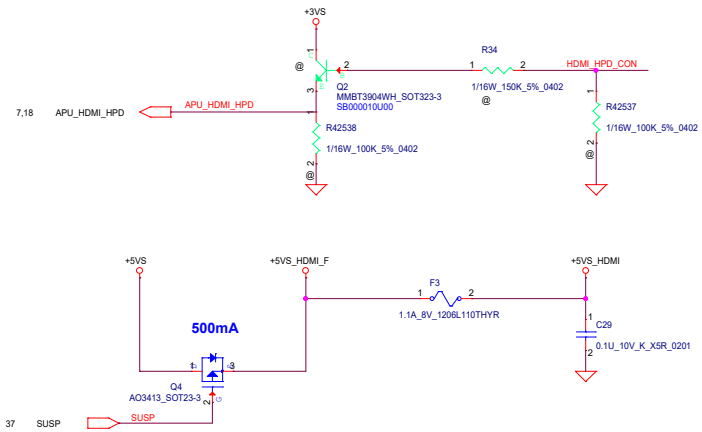
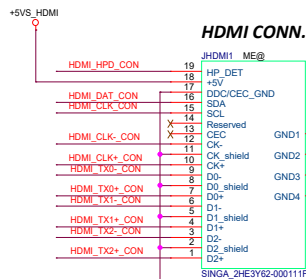
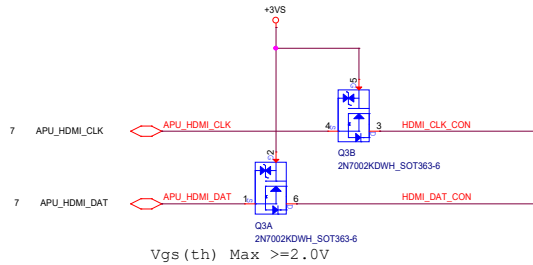
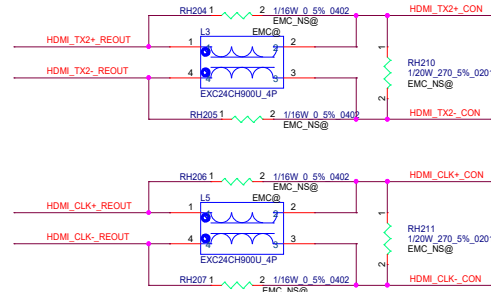
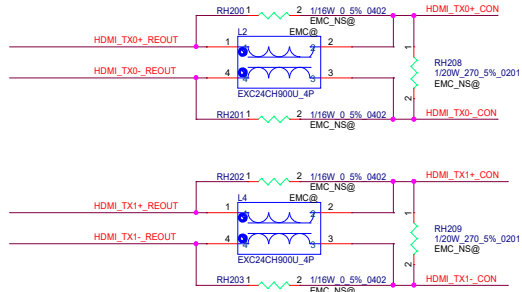
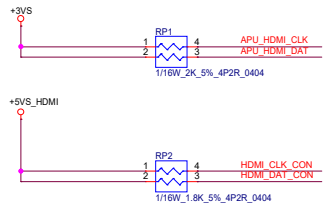
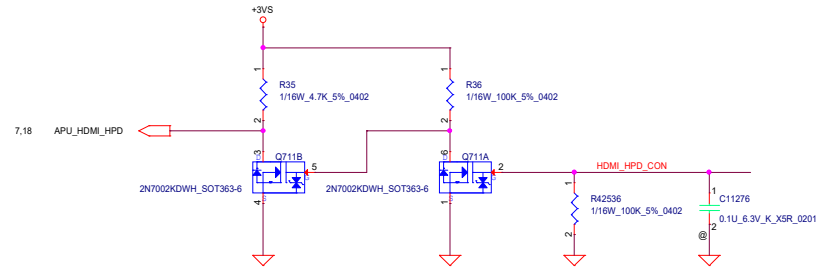
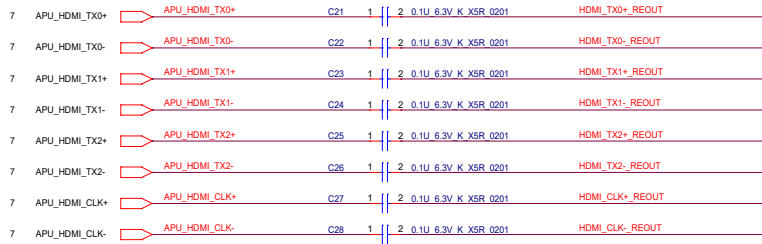
M.2 SSD(M TYPE)



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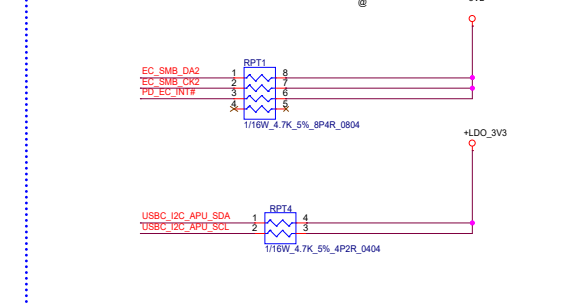
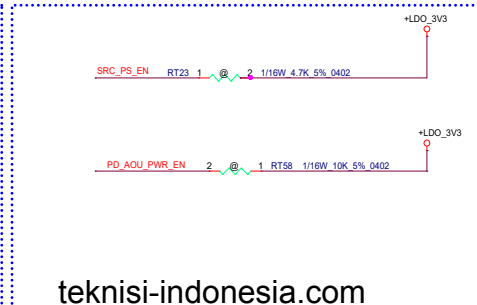
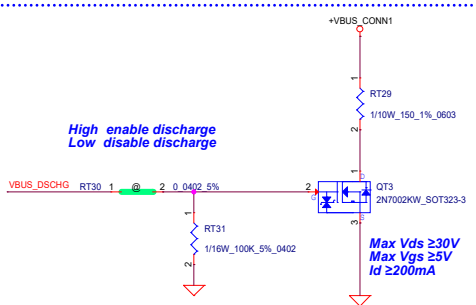
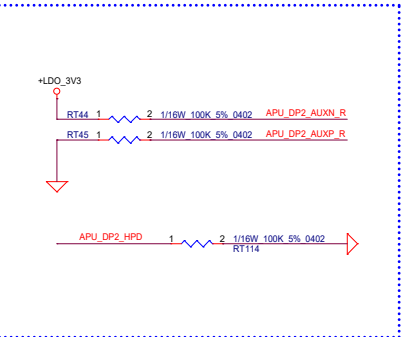
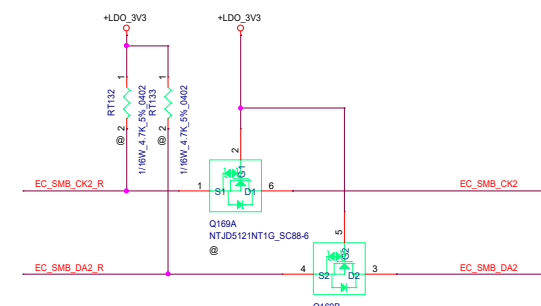
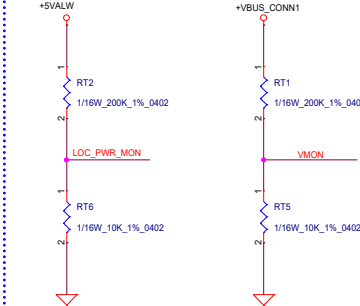
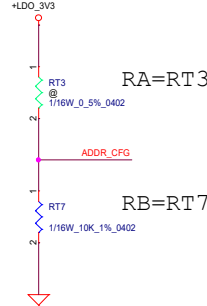




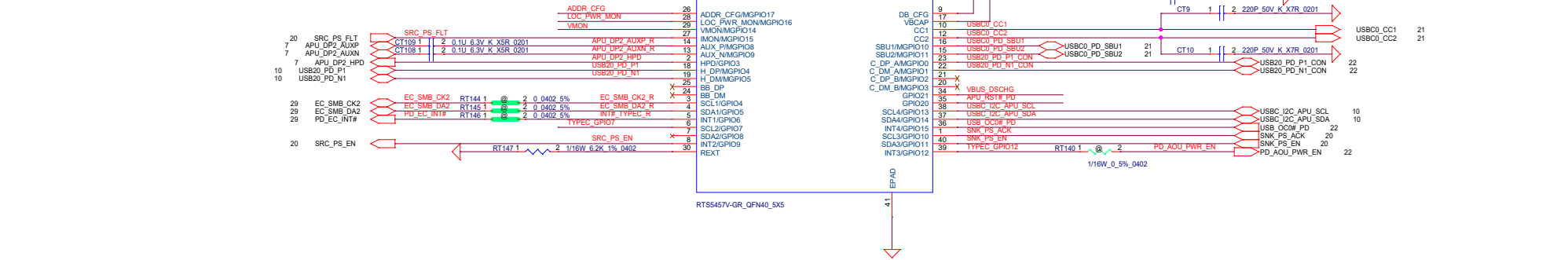
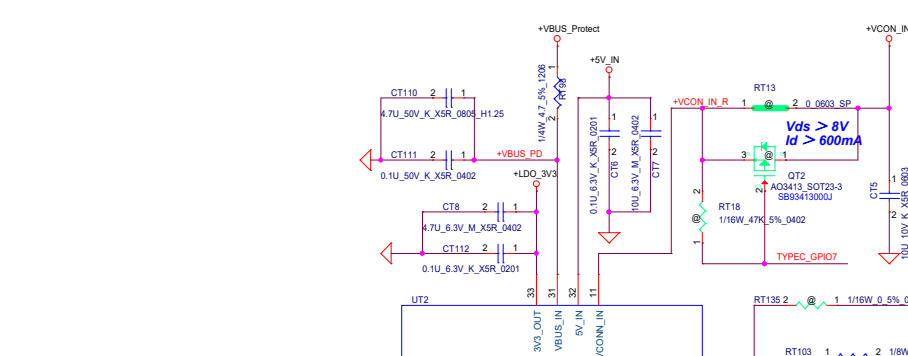
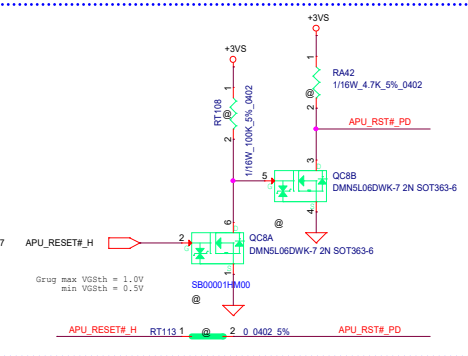


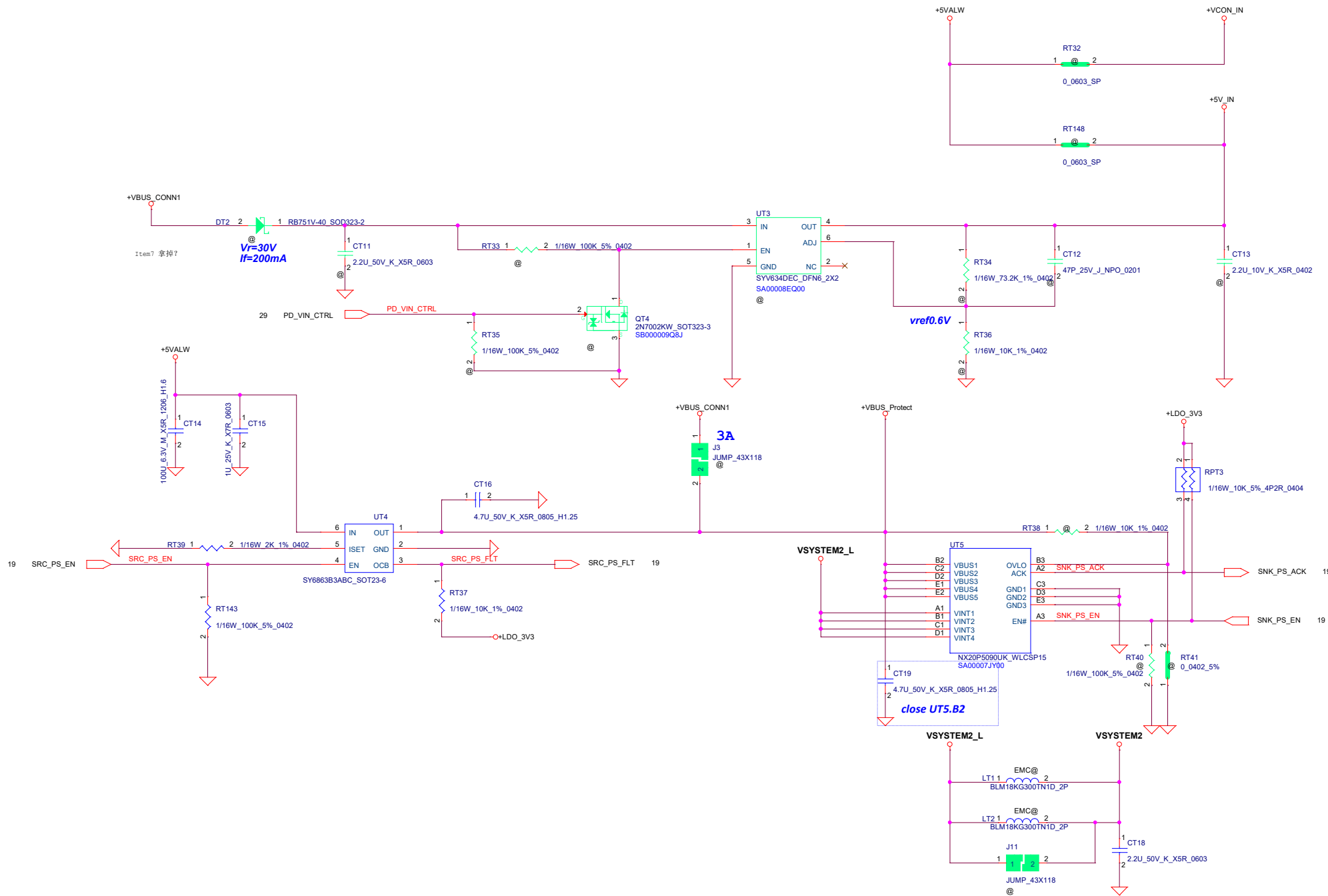
Slave Addr	Ra 5%	Rb 5%	
addr0:0xCC	NC	10K	<0.2V
addr1:0xCE	75K	10K	>=0.2V && <0.6V
addr2:0xD0	33K	10K	>=0.6V && <1.0V
addr3:0xD2	10K	10K	>=1.0V


It's used for SMBUS slave addr0/1/2/3 setting during power on initialization



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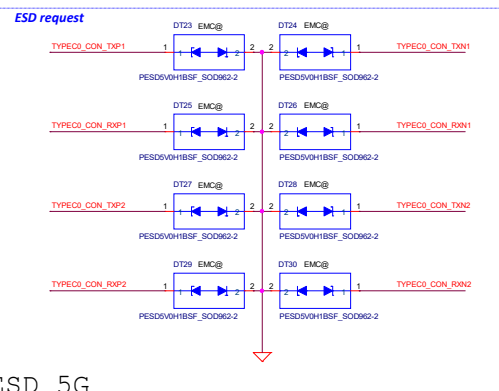
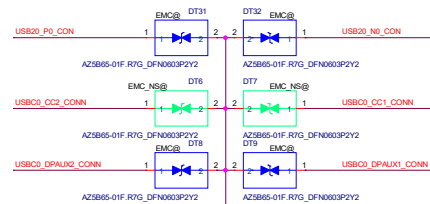
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Issued Date		2019/06/21		Deciphered Date		2019/06/21		PD Power Switch	
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Protect IC

The diagram illustrates a protection circuit for a USB-C PD controller (U7) connected to a USB-A connector (A4). The USB-C connector (UT7) has pins for VBUS, GND, and DP/DM. The VBUS pin is connected to a 5V regulator (U7) and a 10k pull-up resistor (RT28). The GND pin is connected to a 3.3V regulator (U8) and a 10k pull-down resistor (RT101). The DP/DM pins are connected to the USB-C PD controller (U7). The USB-A connector (A4) has pins for VBUS, GND, and DP/DM. The VBUS pin is connected to the 5V regulator (U7) and the 3.3V regulator (U8). The GND pin is connected to ground. The DP/DM pins are connected to the USB-A connector. The circuit is designed to protect the USB-C PD controller from overvoltage and overcurrent during the handshake process.

Legend:

- 1: USB-C PD_SBU1
- 2: USB-C PD_SBU2
- 3: USB-C PD_SBU3
- 4: USB-C PD_SBU4
- 5: USB-C PD_SBU5
- 6: USB-C PD_SBU6
- 7: USB-C PD_SBU7
- 8: USB-C PD_SBU8
- 9: USB-C PD_SBU9
- 10: USB-C PD_SBU10
- 11: USB-C PD_SBU11
- 12: USB-C PD_SBU12
- 13: USB-C PD_SBU13
- 14: USB-C PD_SBU14
- 15: USB-C PD_SBU15
- 16: USB-C PD_SBU16
- 17: USB-C PD_SBU17
- 18: USB-C PD_SBU18
- 19: USB-C PD_SBU19
- 20: USB-C PD_SBU20
- 21: USB-C PD_SBU21
- 22: USB-C PD_SBU22
- 23: USB-C PD_SBU23
- 24: USB-C PD_SBU24
- 25: USB-C PD_SBU25
- 26: USB-C PD_SBU26
- 27: USB-C PD_SBU27
- 28: USB-C PD_SBU28
- 29: USB-C PD_SBU29
- 30: USB-C PD_SBU30
- 31: USB-C PD_SBU31
- 32: USB-C PD_SBU32
- 33: USB-C PD_SBU33
- 34: USB-C PD_SBU34
- 35: USB-C PD_SBU35
- 36: USB-C PD_SBU36
- 37: USB-C PD_SBU37
- 38: USB-C PD_SBU38
- 39: USB-C PD_SBU39
- 40: USB-C PD_SBU40
- 41: USB-C PD_SBU41
- 42: USB-C PD_SBU42
- 43: USB-C PD_SBU43
- 44: USB-C PD_SBU44
- 45: USB-C PD_SBU45
- 46: USB-C PD_SBU46
- 47: USB-C PD_SBU47
- 48: USB-C PD_SBU48
- 49: USB-C PD_SBU49
- 50: USB-C PD_SBU50
- 51: USB-C PD_SBU51
- 52: USB-C PD_SBU52
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- 63: USB-C PD_SBU63
- 64: USB-C PD_SBU64
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- 70: USB-C PD_SBU70
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- 72: USB-C PD_SBU72
- 73: USB-C PD_SBU73
- 74: USB-C PD_SBU74
- 75: USB-C PD_SBU75
- 76: USB-C PD_SBU76
- 77: USB-C PD_SBU77
- 78: USB-C PD_SBU78
- 79: USB-C PD_SBU79
- 80: USB-C PD_SBU80
- 81: USB-C PD_SBU81
- 82: USB-C PD_SBU82
- 83: USB-C PD_SBU83
- 84: USB-C PD_SBU84
- 85: USB-C PD_SBU85
- 86: USB-C PD_SBU86
- 87: USB-C PD_SBU87
- 88: USB-C PD_SBU88
- 89: USB-C PD_SBU89
- 90: USB-C PD_SBU90
- 91: USB-C PD_SBU91
- 92: USB-C PD_SBU92
- 93: USB-C PD_SBU93
- 94: USB-C PD_SBU94
- 95: USB-C PD_SBU95
- 96: USB-C PD_SBU96
- 97: USB-C PD_SBU97
- 98: USB-C PD_SBU98
- 99: USB-C PD_SBU99
- 100: USB-C PD_SBU100



USB0_C1_CONN

CT113

EMC NS@

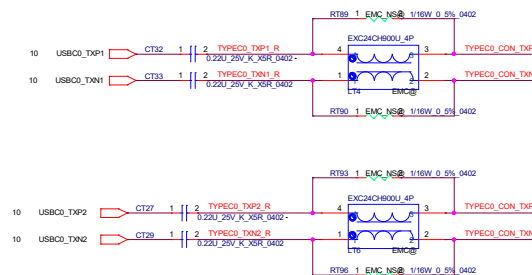
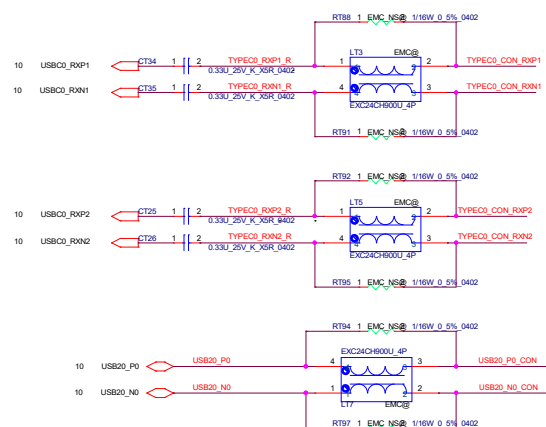
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USB0_C2_CONN

CT114


EMC NS@

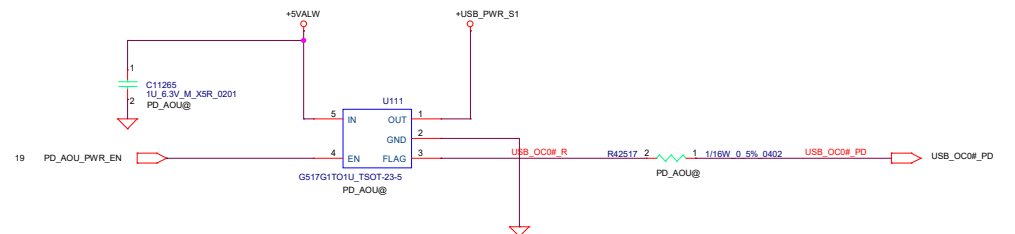
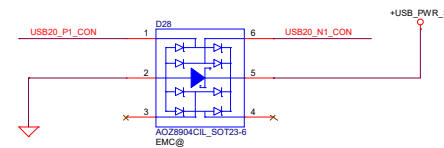
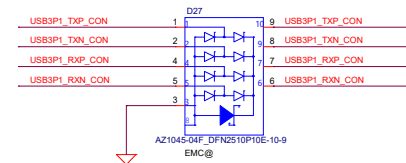
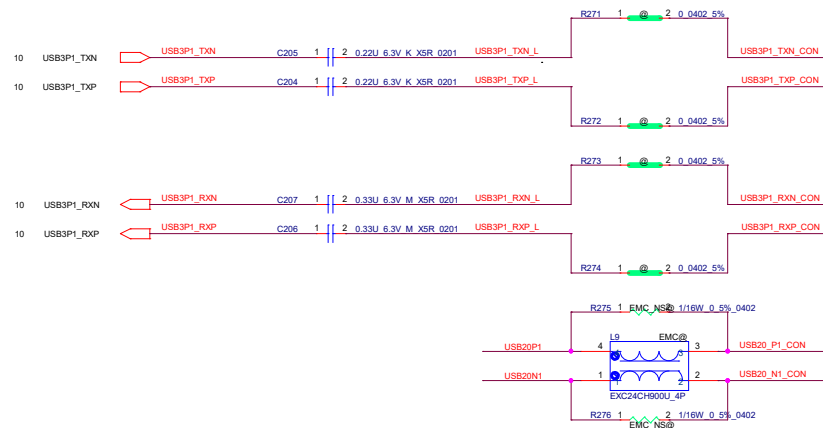
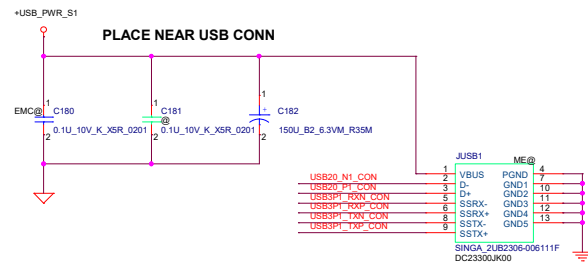
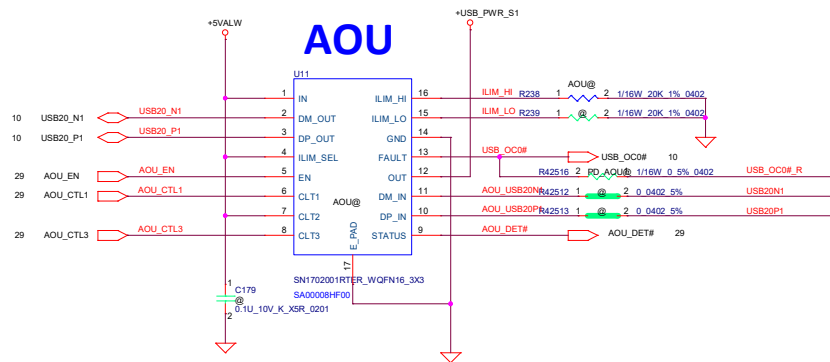
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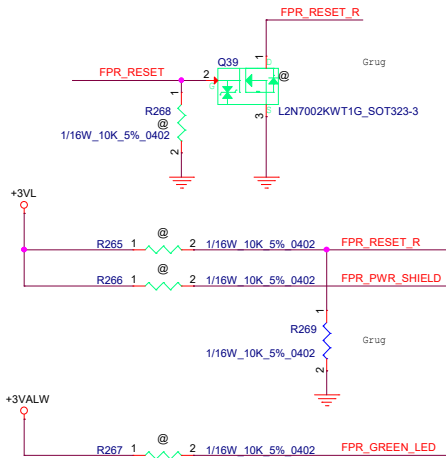
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C Connector

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Date	Monday, February 01, 2021					

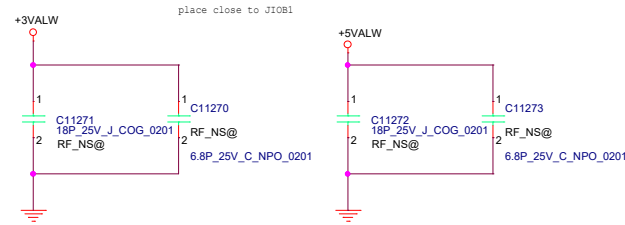


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Board ID for FPR support

	NON-FPR	FPR
FPR_STUFF_CTL	leave as NC	Connect to GND by FPR IO board

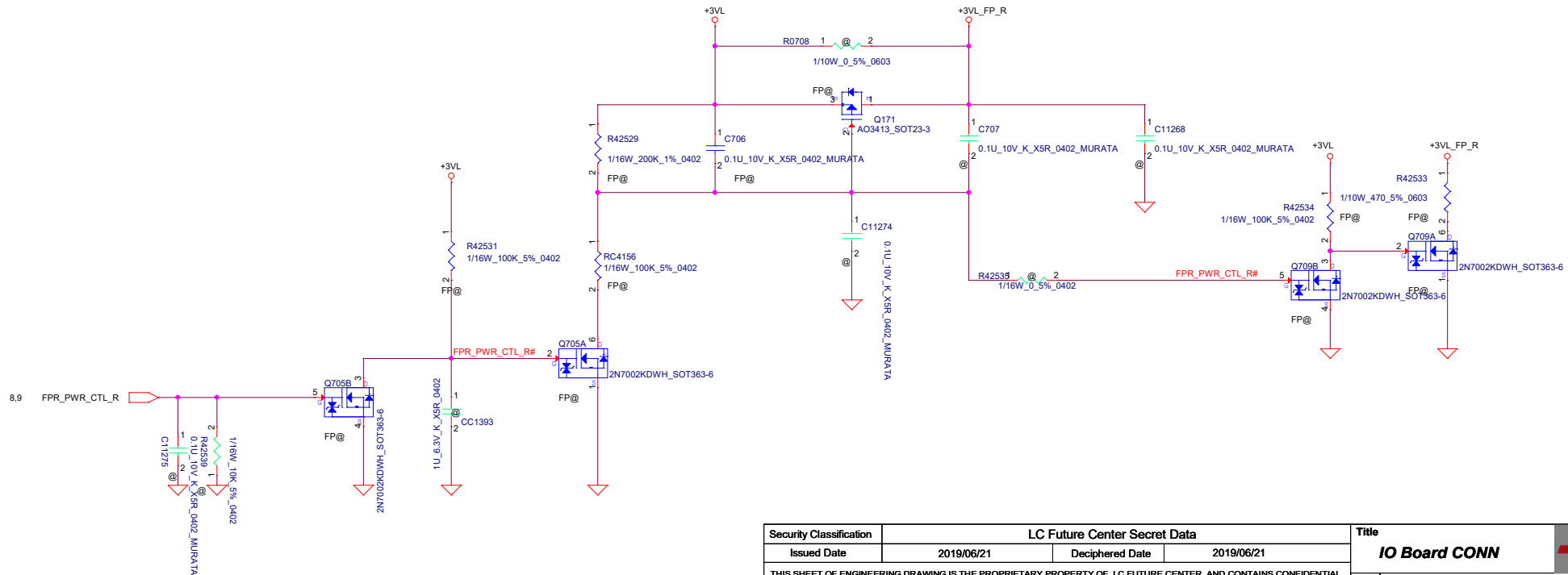
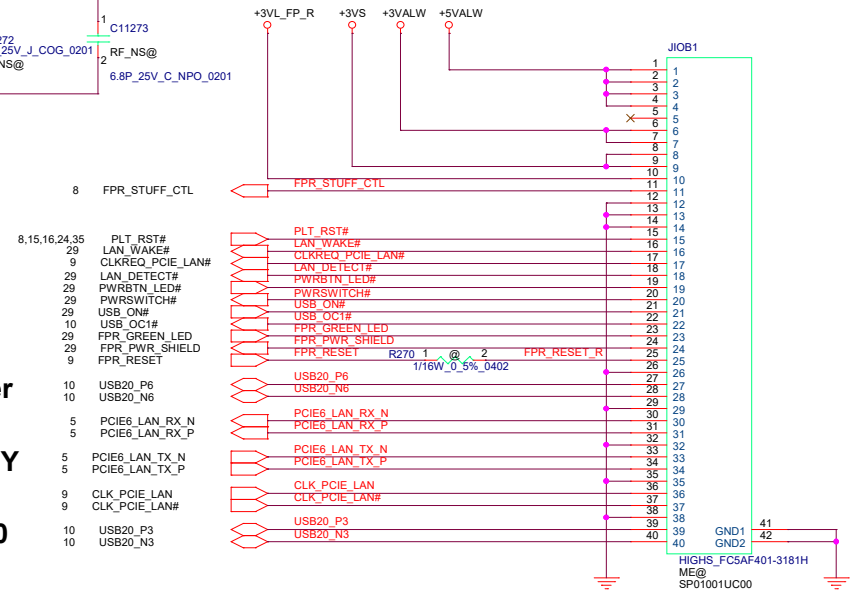


Finger Printer

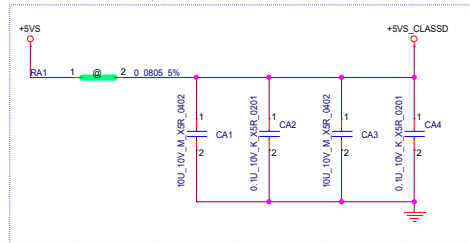
GBE LAN PHY

USB 2.0

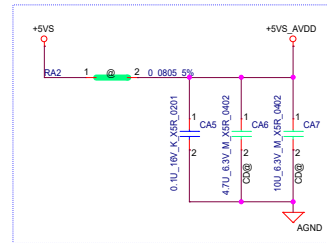
IO_40_Pin conn



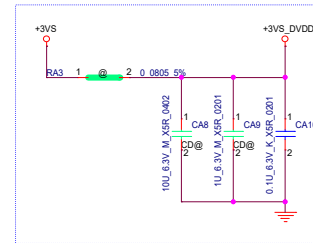
Close to Pin41,46



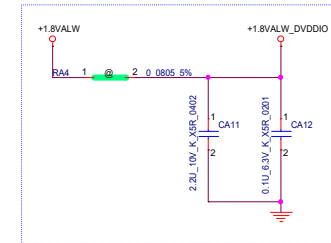
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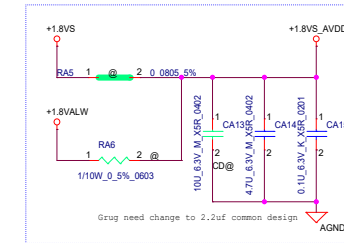
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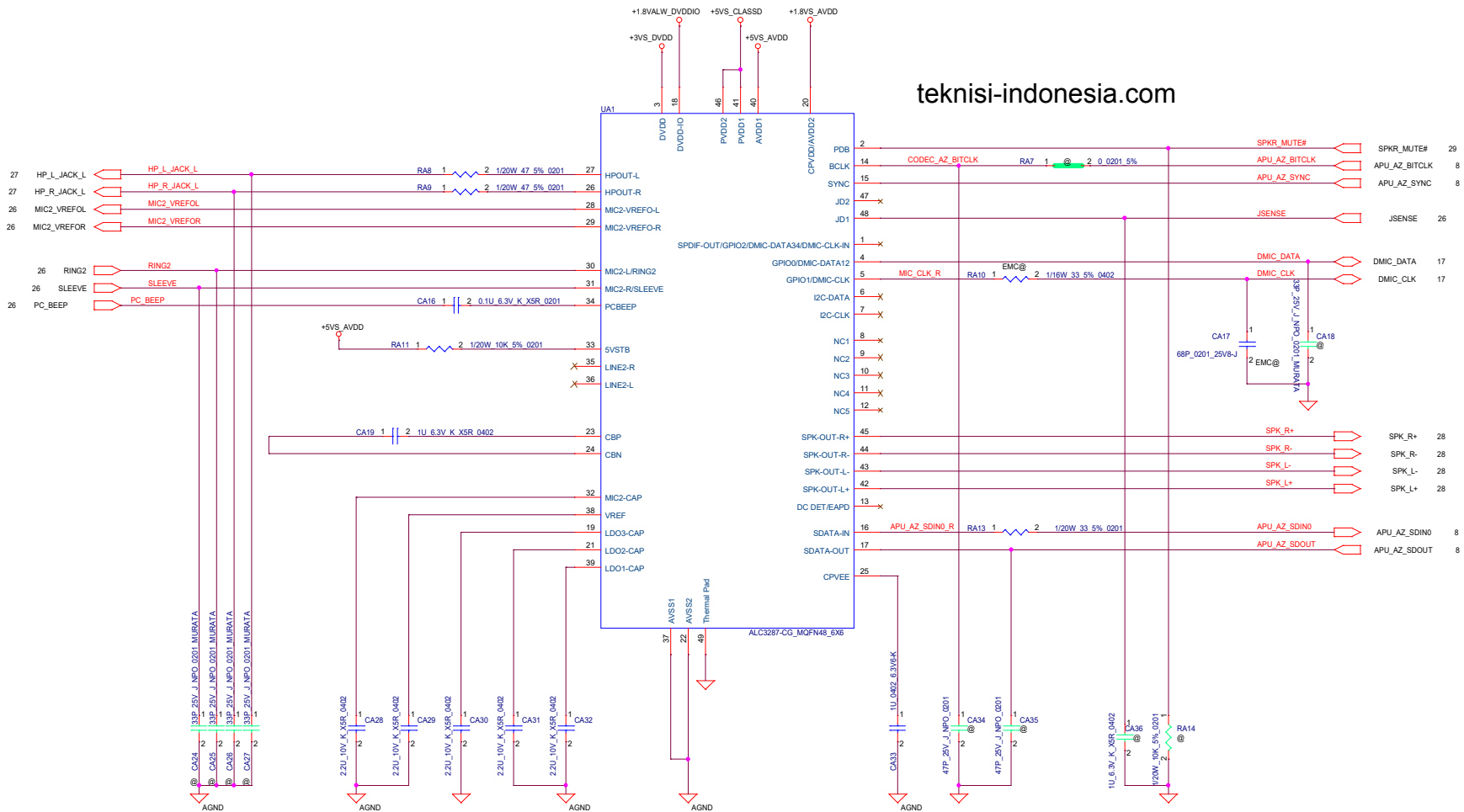
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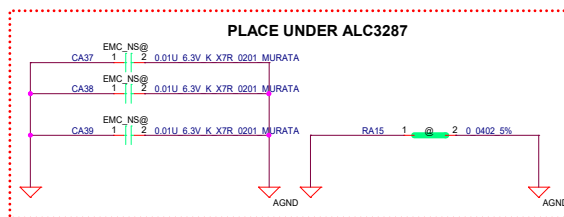
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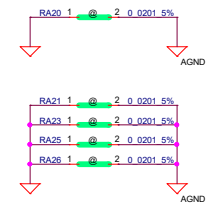
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PLACE UNDER ALC3287



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		Sheet 25 of 50		



EC Beep

29 BEEP#

PCH Beep

8 PCH_BEEP

PC_BEEP

29

2

1/16W_4.7K_5%_0402

RA29

1 2

CA44 1 2 0.1U 10V K_XSR_0201

PC_BEEP_MUX1

R42518

2 0.0201_5%

PC_BEEP

2

1/16W_4.7K_5%_0402

RA35

1 2

CA45 1 2 0.1U 10V K_XSR_0201

+3V_ALW

R42519

1/16W_100K_5%_0402

Q38

LSK3541G1ET2L_VMT3

Q170


LSK3541G1ET2L_VMT3

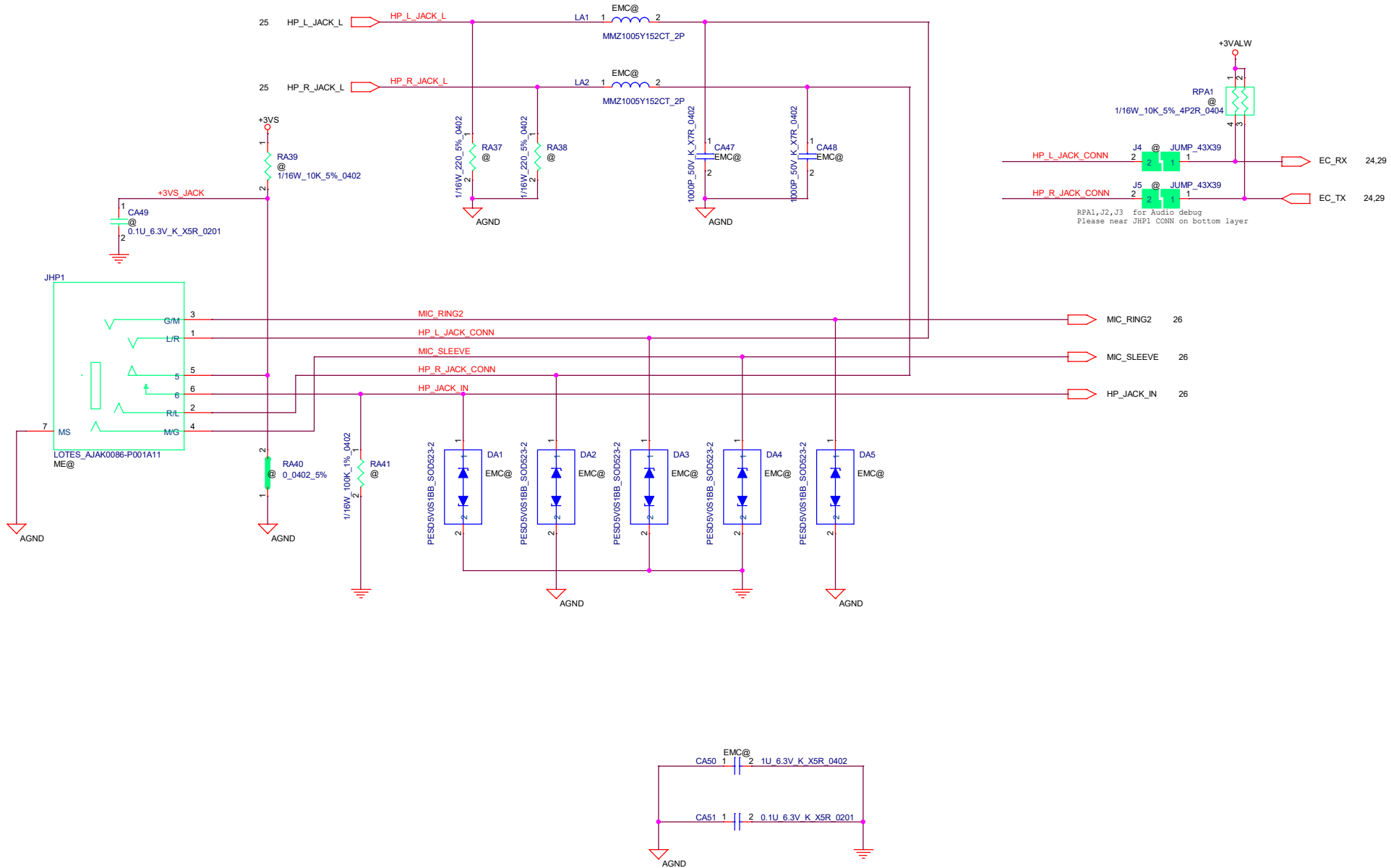
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29

1

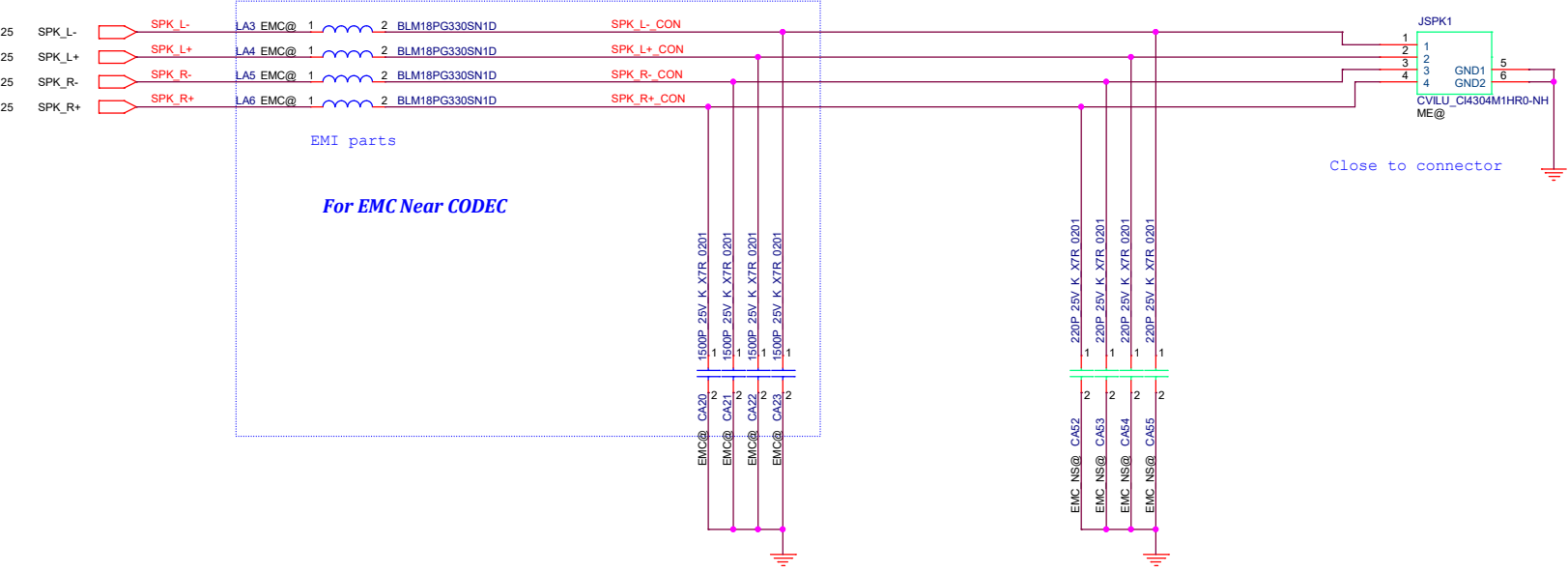


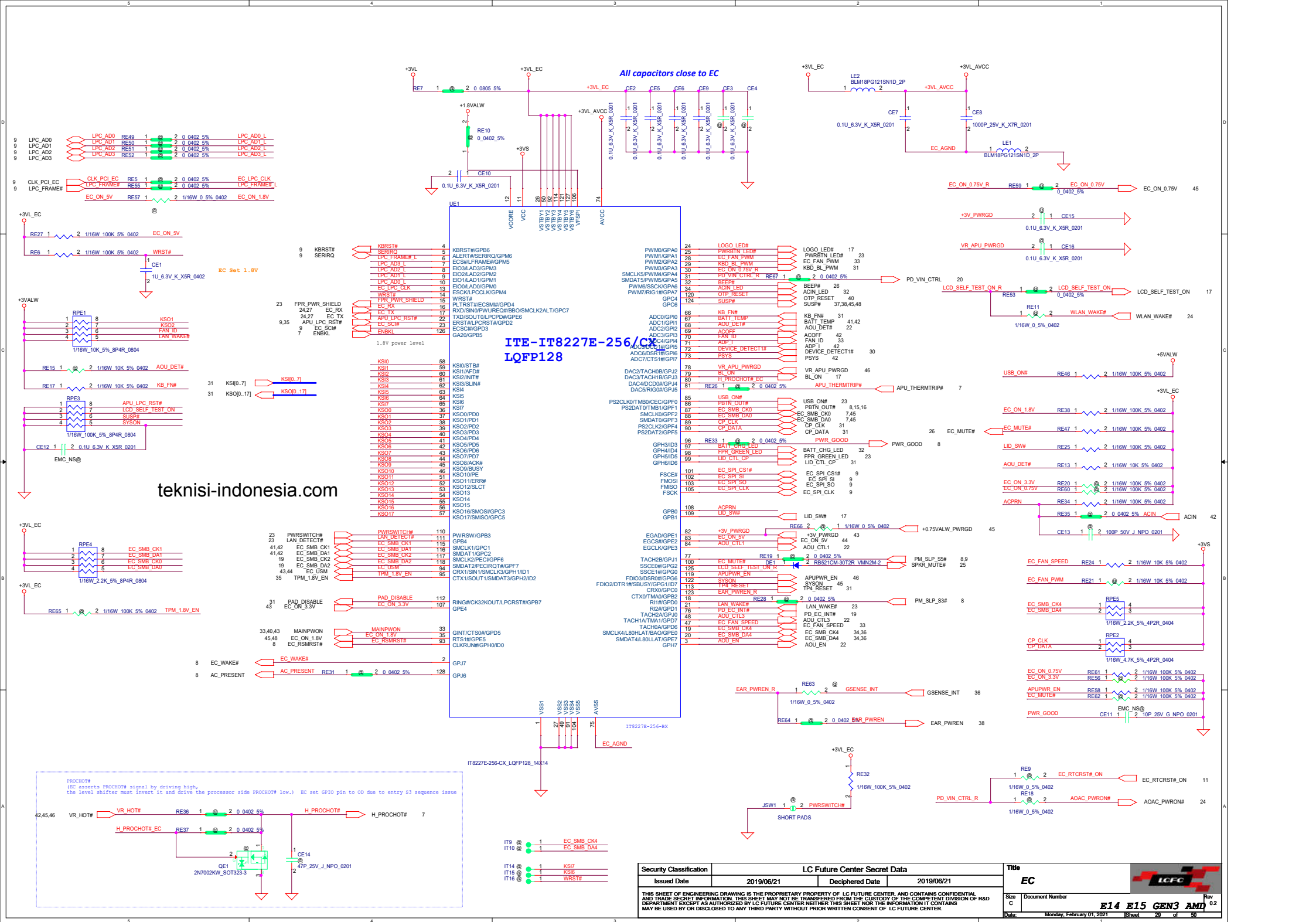
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Date				Monday, February 01, 2021	Sheet	26	of 50



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Custom	E14 E15 GEN3 AMD					
Date:	Monday, February 01, 2021		Sheet	27	of	50

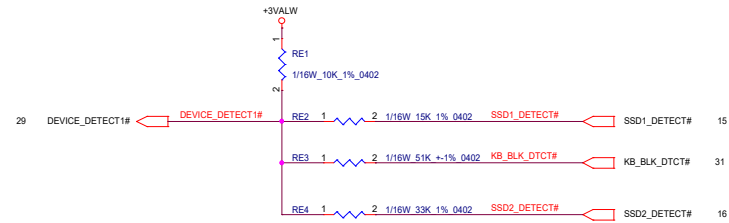
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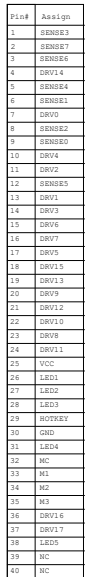
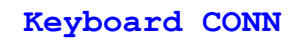
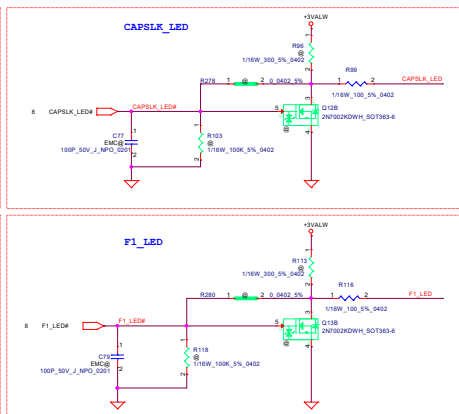


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Vcc	3.3V					
RE1	10K +/- 5%					
DEVICE_DETECT1#	1.98V	1.675V	1.772V	2.759V	2.533V	3.3V
SSD1_DETECT#	V	V	V	X	X	X
KB_BLK_DTCT#	X	V	X	X	V	X
SSD2_DETECT#	X	X	V	V	X	X

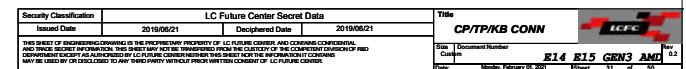
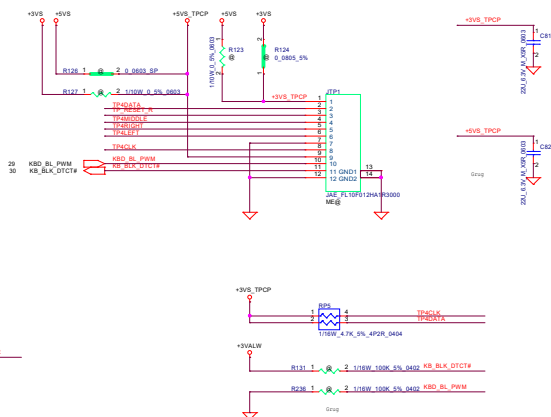


Assign	Purpose
VCC	Vcc 3V for LED
LED1	LED for Fn
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLK
LED5	LED for NumLock

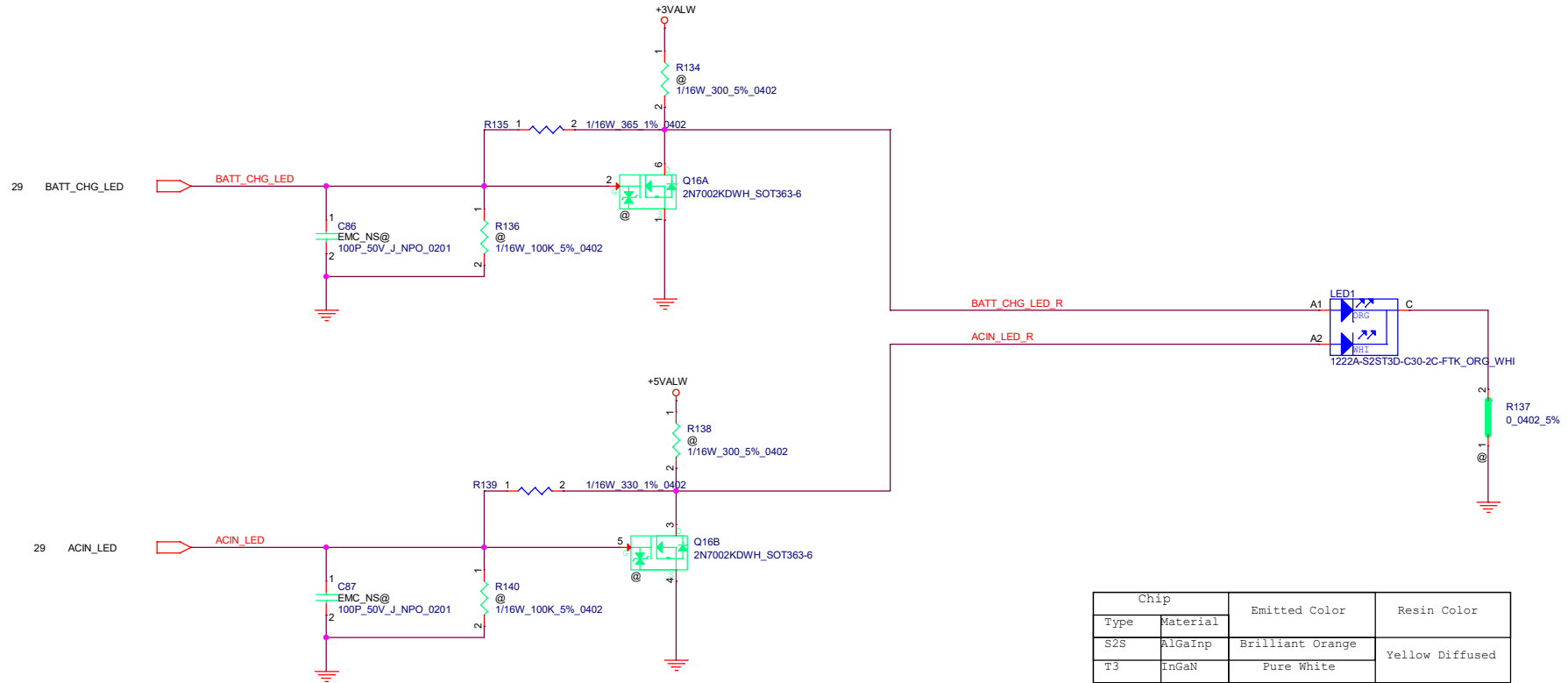
Assign	Purpose
MC	Common pin for TrackPoint click button
M1	Left button
M2	Right button
M3	Center button




Pin #	Assign
1	VCC5 (5V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	BL detection
12	LED GND



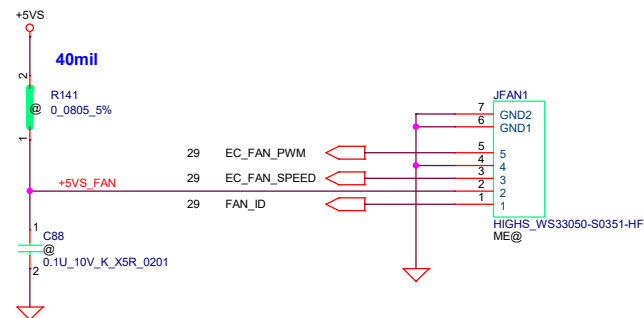
POWER ADAPTER Bi-COLOR (ORANGE/WHITE)



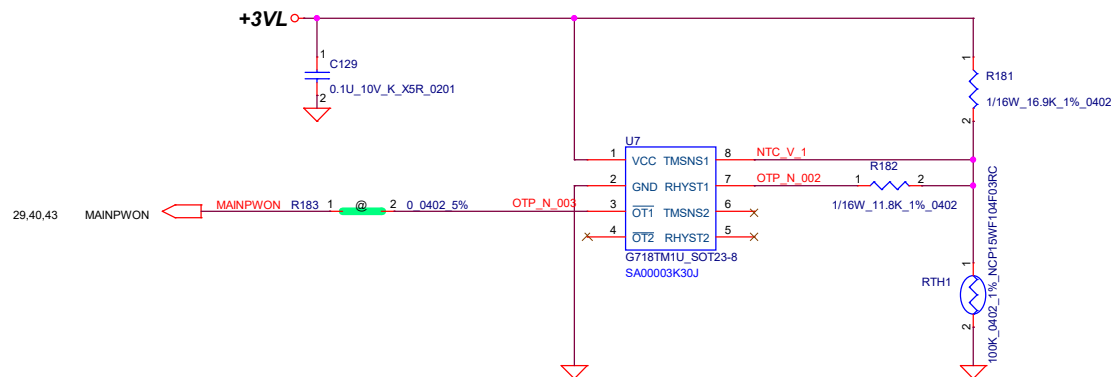
Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInp	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	

Security Classification		LC Future Center Secret Data		Title					
Issued Date	2019/06/21	Deciphered Date	2019/06/21	Power LED					
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FAN CONN.



HW Protect

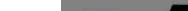


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over temperature threshold:
RSET=3*RTMH
100+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
80+/-30C

```

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Thermal Sensor

1 Near

2 Remote

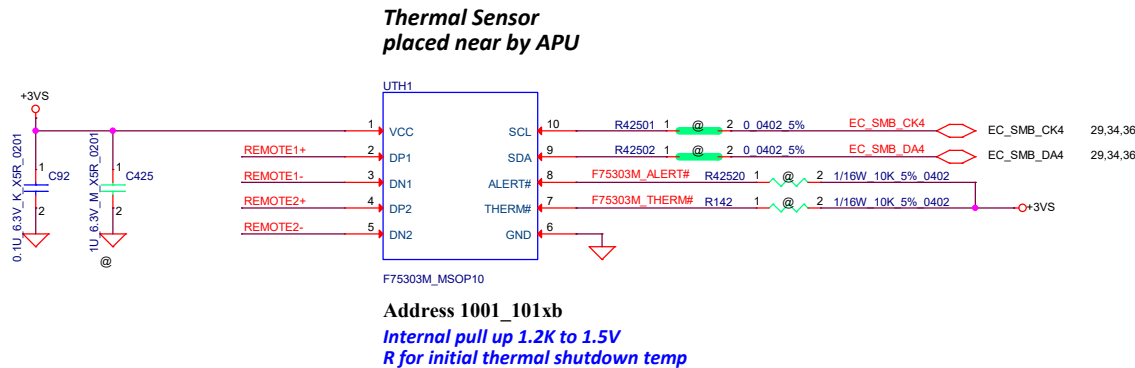
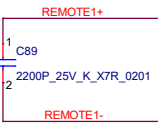
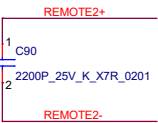


TABLE of Thermal Sensor (UTH1)		
Vendor	LCFC P/N	Description
FINTEK	SA000046C0J	S IC F75303M MSOP 10P SENSOR

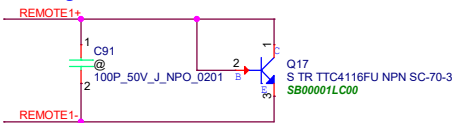
Near UTH1



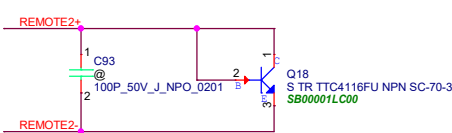
Near UTH1



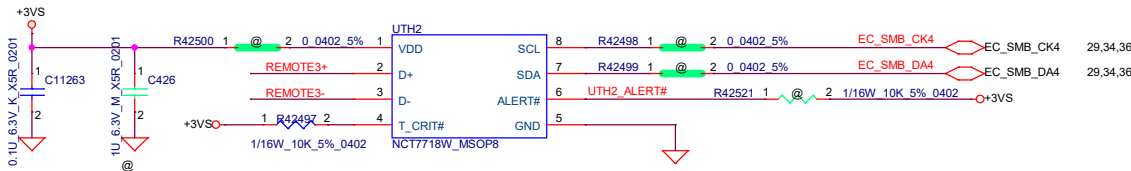
Near Charger



Near Fin

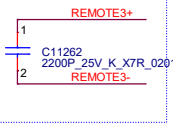


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

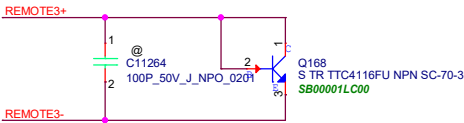


NCT7718W I2
C/ SMBus™ address is 1001100xb (x is R/W bit).

Close to UTH2



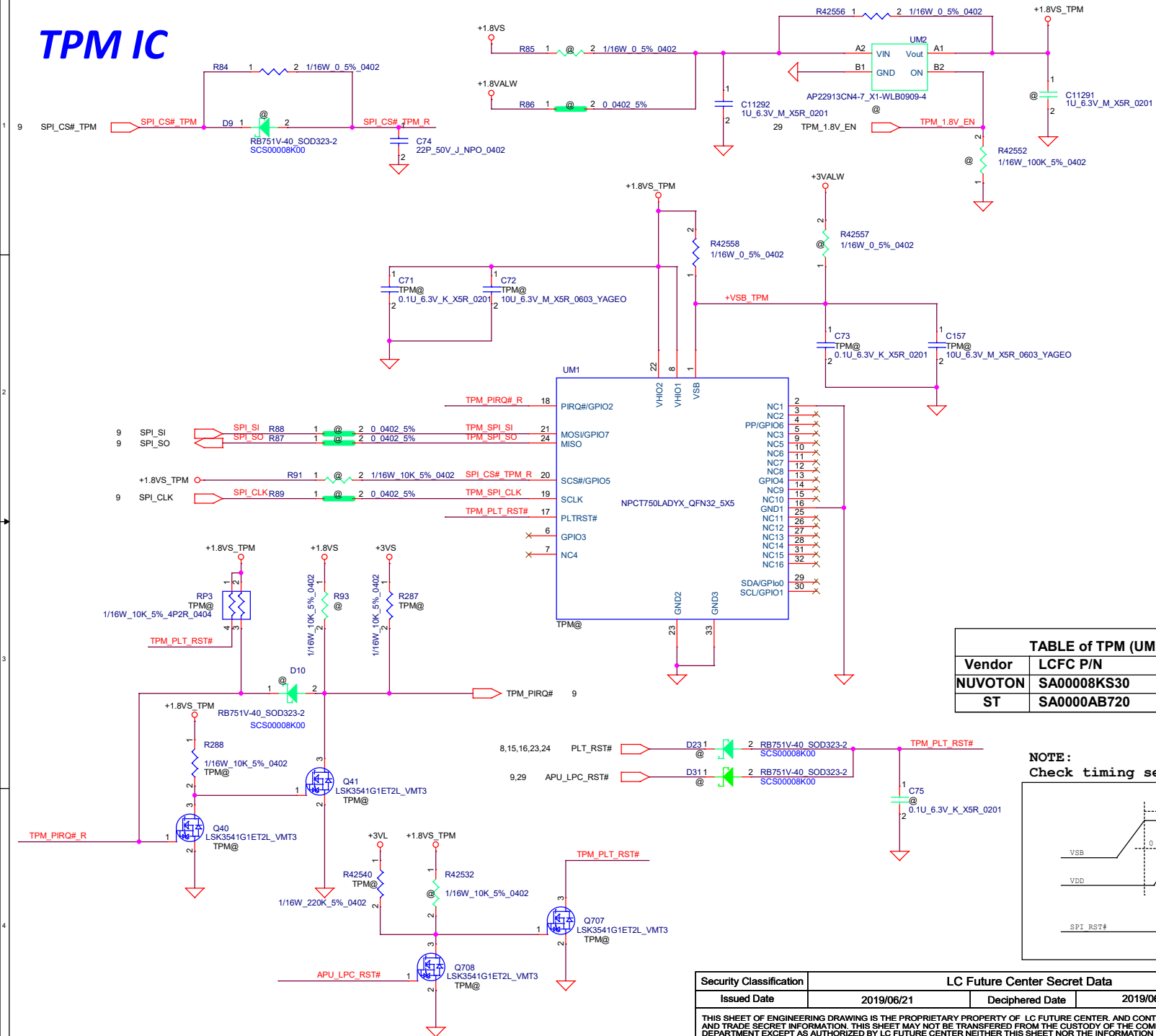
Near



REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

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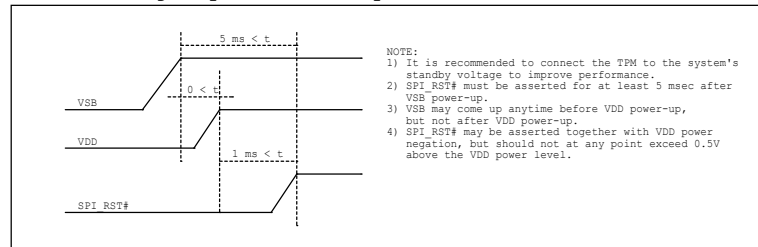
TPM IC




Pin	PTP Spec	NUVOTON NFC750LADYX	ST ST33HTPH2X32AHD8
1	VSB	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	PP/GPIO6	PP/GPIO6	NC
5	NC	NC	NC
6	GPI03	GPI03	NC
7	PP	NC	PP
8	VHIO	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPI04	GPI04	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_IRQ#	PIRQ#/GPIO2	SPI_IRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#/CPI05	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO0	SDA/GPIO0	NC
30	SCL/GPIO1	SCL/GPIO1	NC
31	NC	NC	NC
32	NC	NC	NC

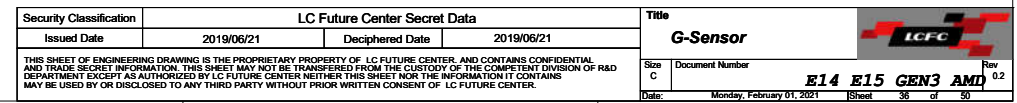
TABLE of TPM (UM1)		
Vendor	LCFC P/N	Description
NUVOTON	SA00008KS30	S IC NPCT750LADYX QFN 32P TPM 2.0
ST	SA0000AB720	S IC ST33HTPH2X32AHD8 VQFN 32P TPM 2.0

NOTE:
Check timing sequence in SDV phase.



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P/N	ADDR_SEL	Address
LIS2DWLTR	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
BMA280	H L	32h (W) & 33h (R) 30h (W) & 31h (R)



+3VS load Switch

+3VALW to +3VS 6.2A request
V9B+ 9V--13V

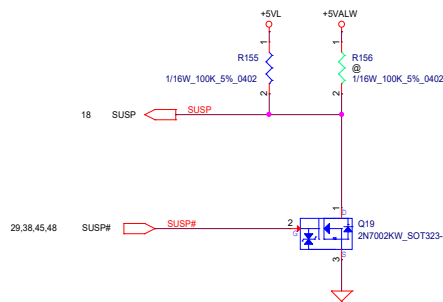
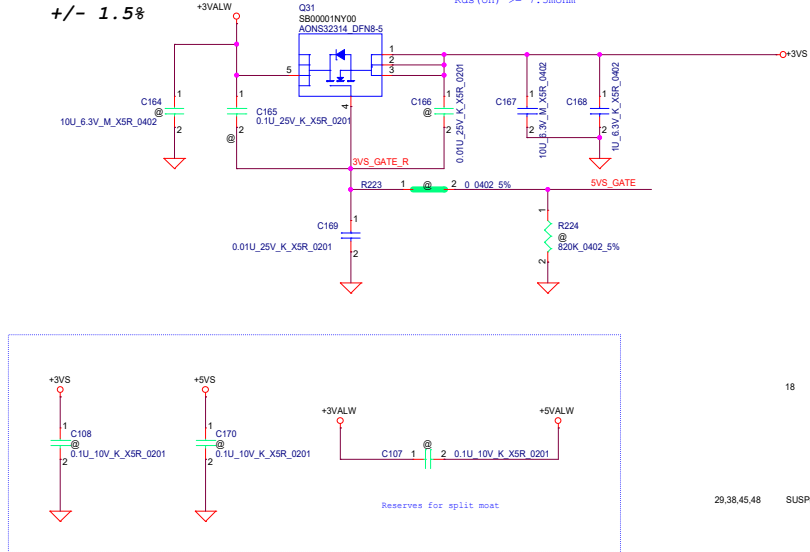
+5VS load Switch

+5VALW to +5VS 2.6A request

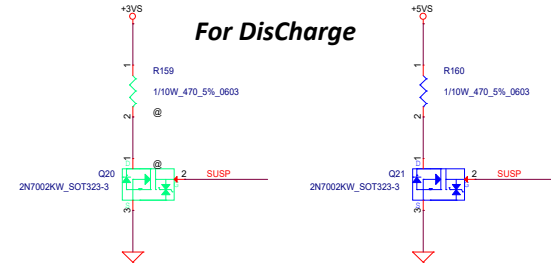
Load MOS N MOS Id <= 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm

+/- 1.5%

+/- 1.5%



For DisCharge



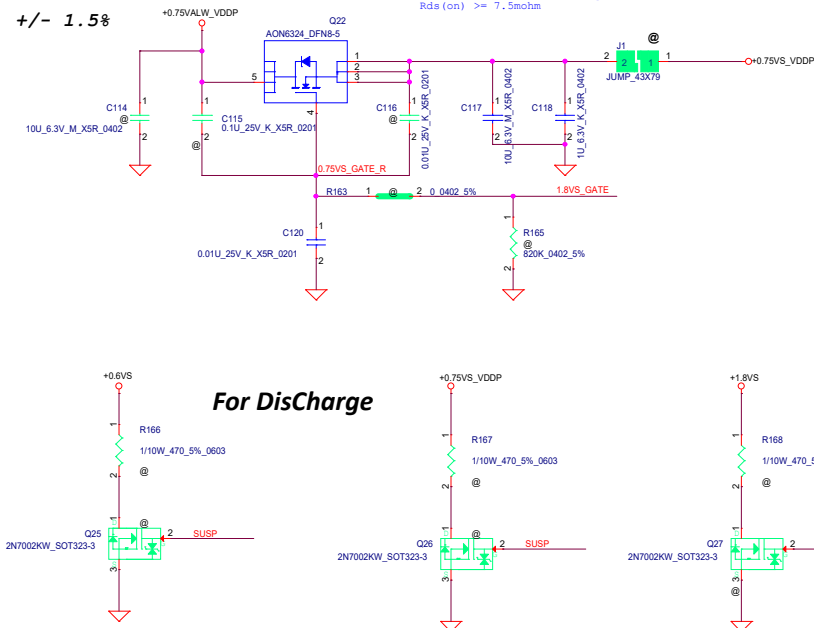
+VDDP load Switch

+0.75VALW_VDDP to +0.75VDDP 10A request
V9B+ 9V--13V

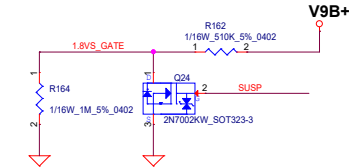
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+/- 1.5%

Load MOS N MOS Id <= 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm

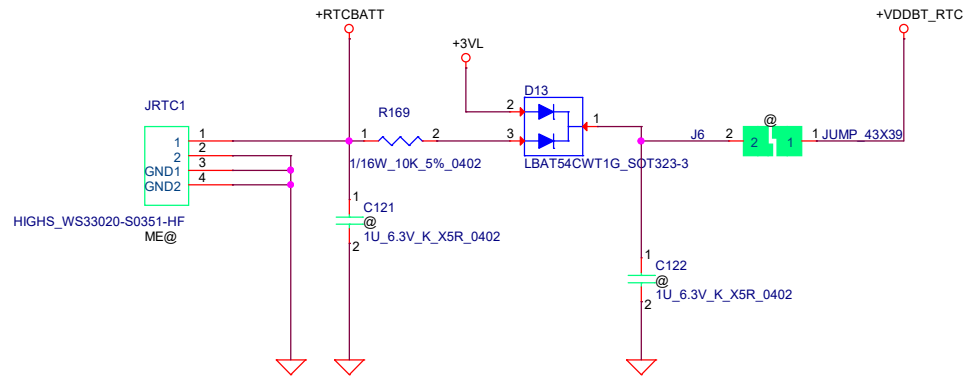


For DisCharge

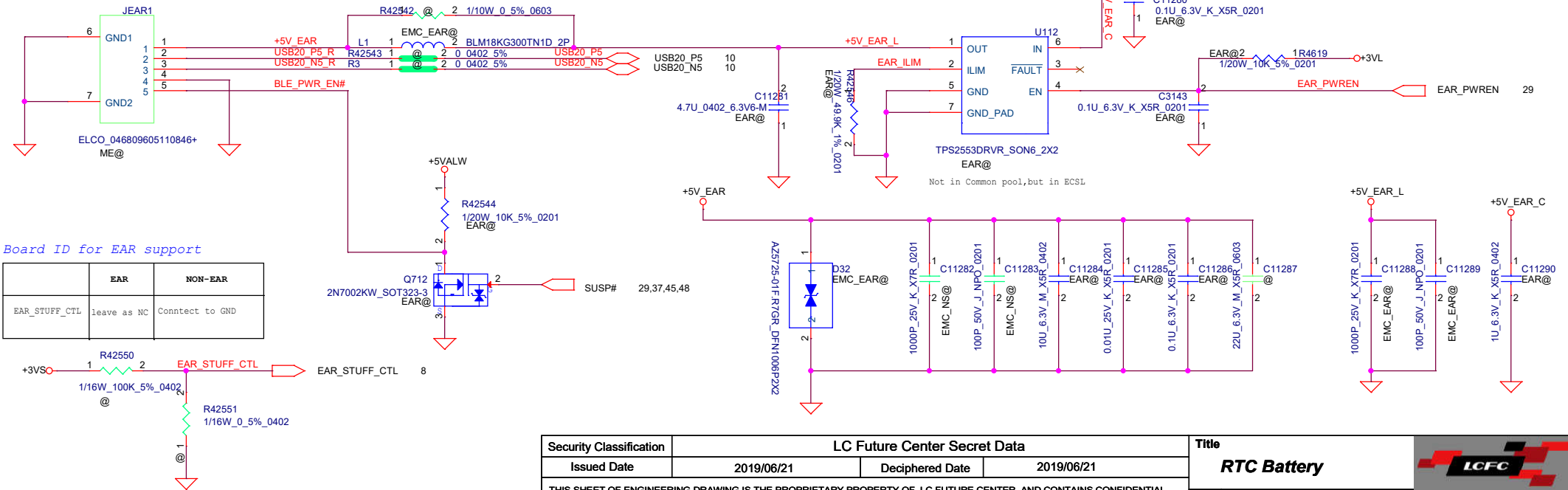


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RTC BATTERY



EARPHONE CHARGE

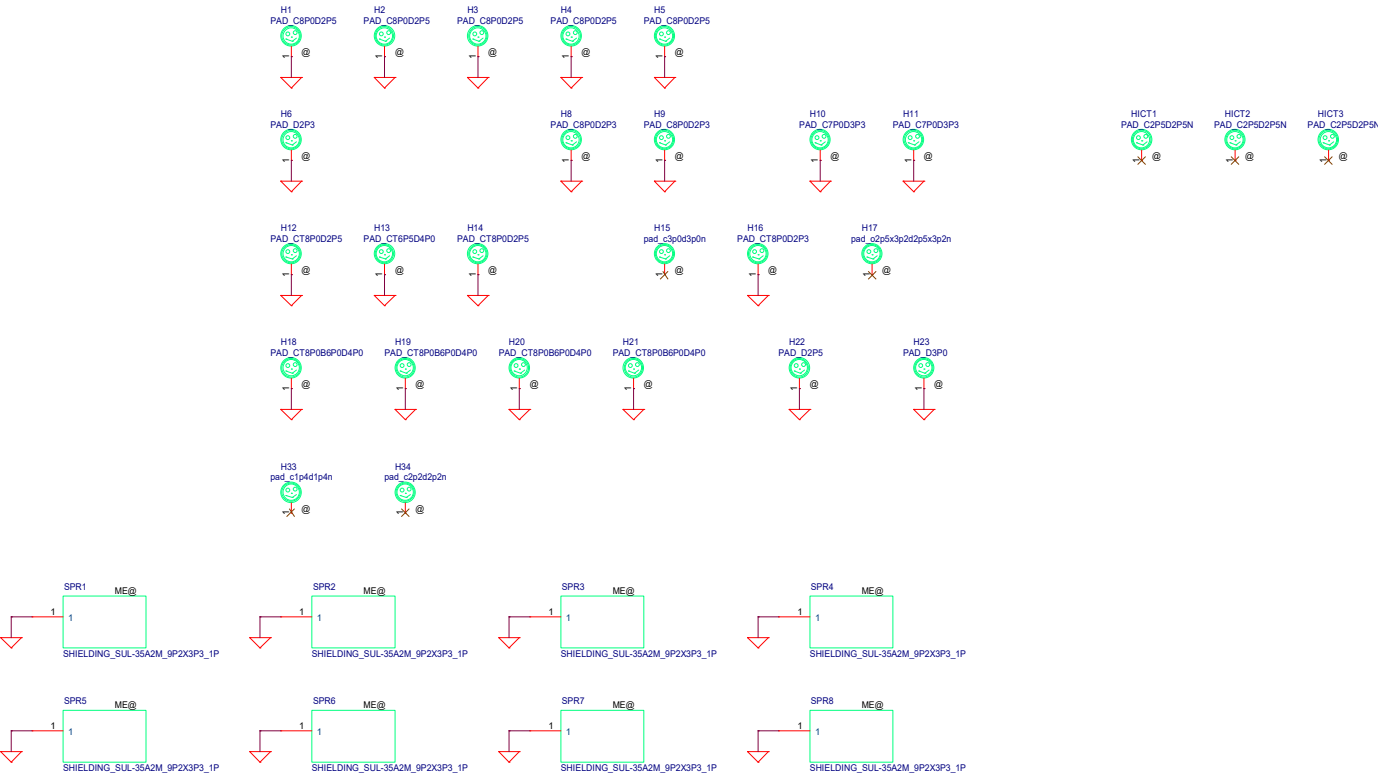


Board ID for EAR support

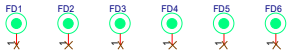
	EAR	NON-EAR
EAR_STUFF_CTL	leave as NC	Connect to GND

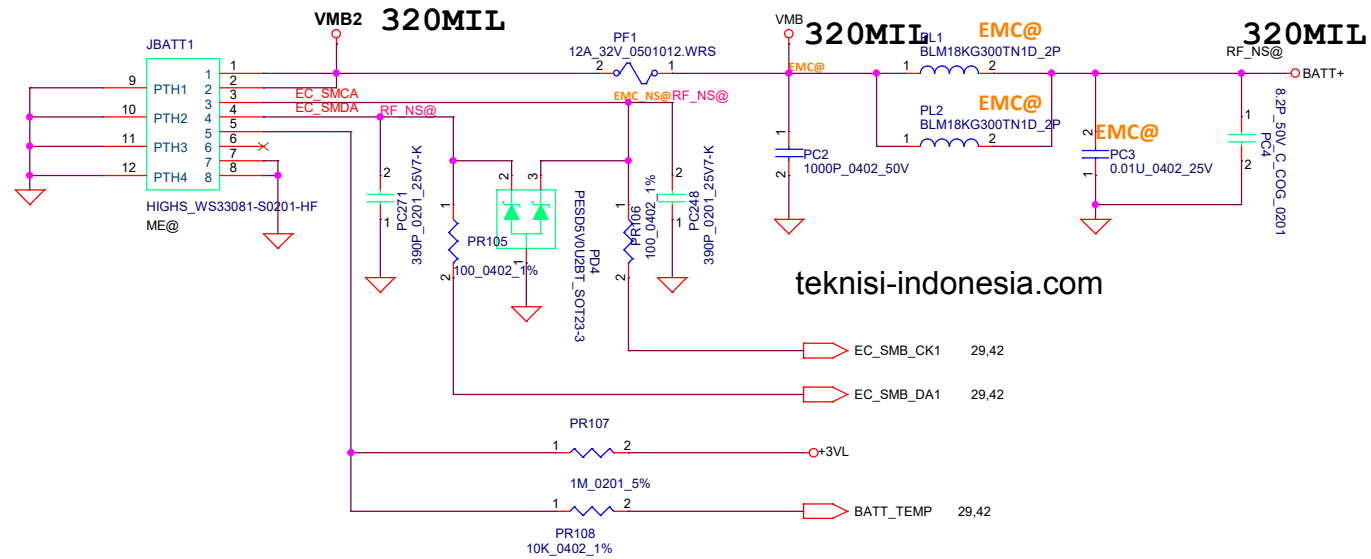
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Screw Hole



PCB Fedical Mark PAD





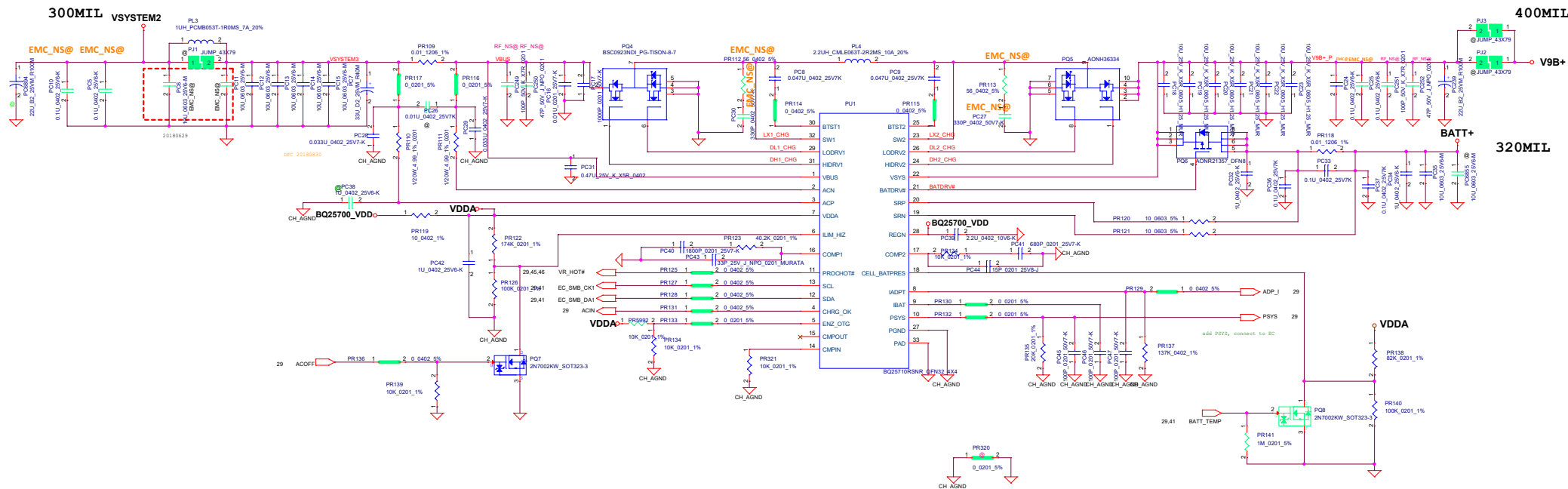
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<Variant Name>

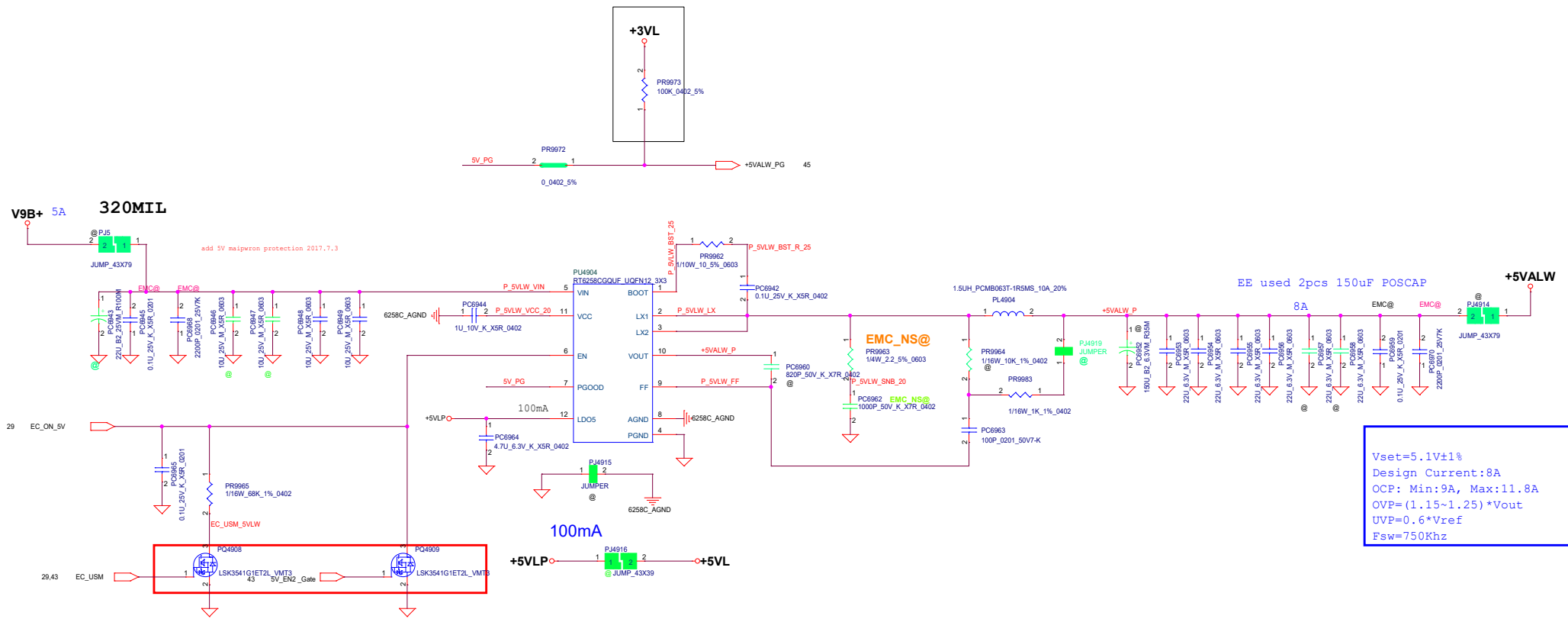
Security Classification	LC Future Center Secret Data		
Issued Date	2018/03/26	Deciphered Date	2019/06/01
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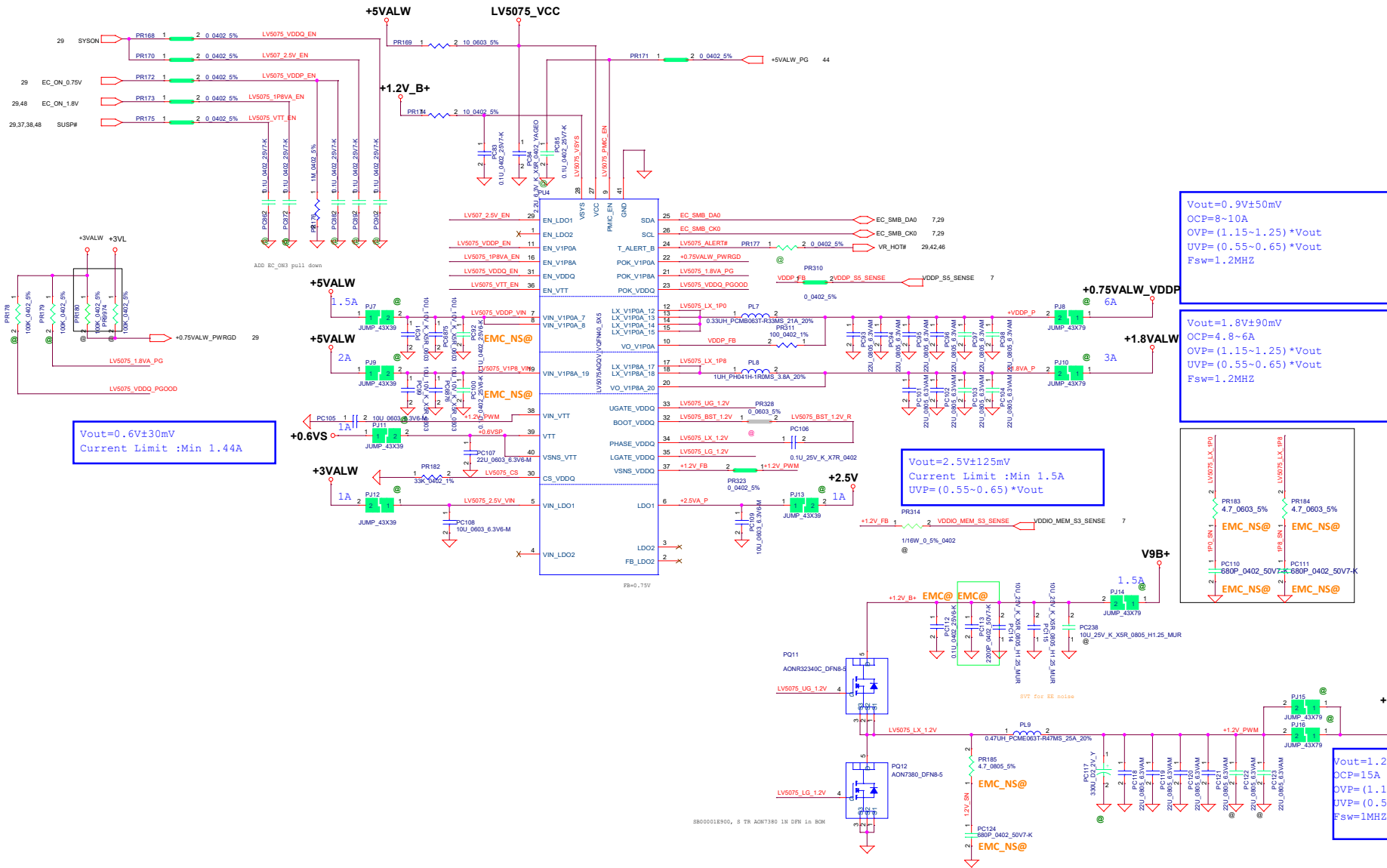


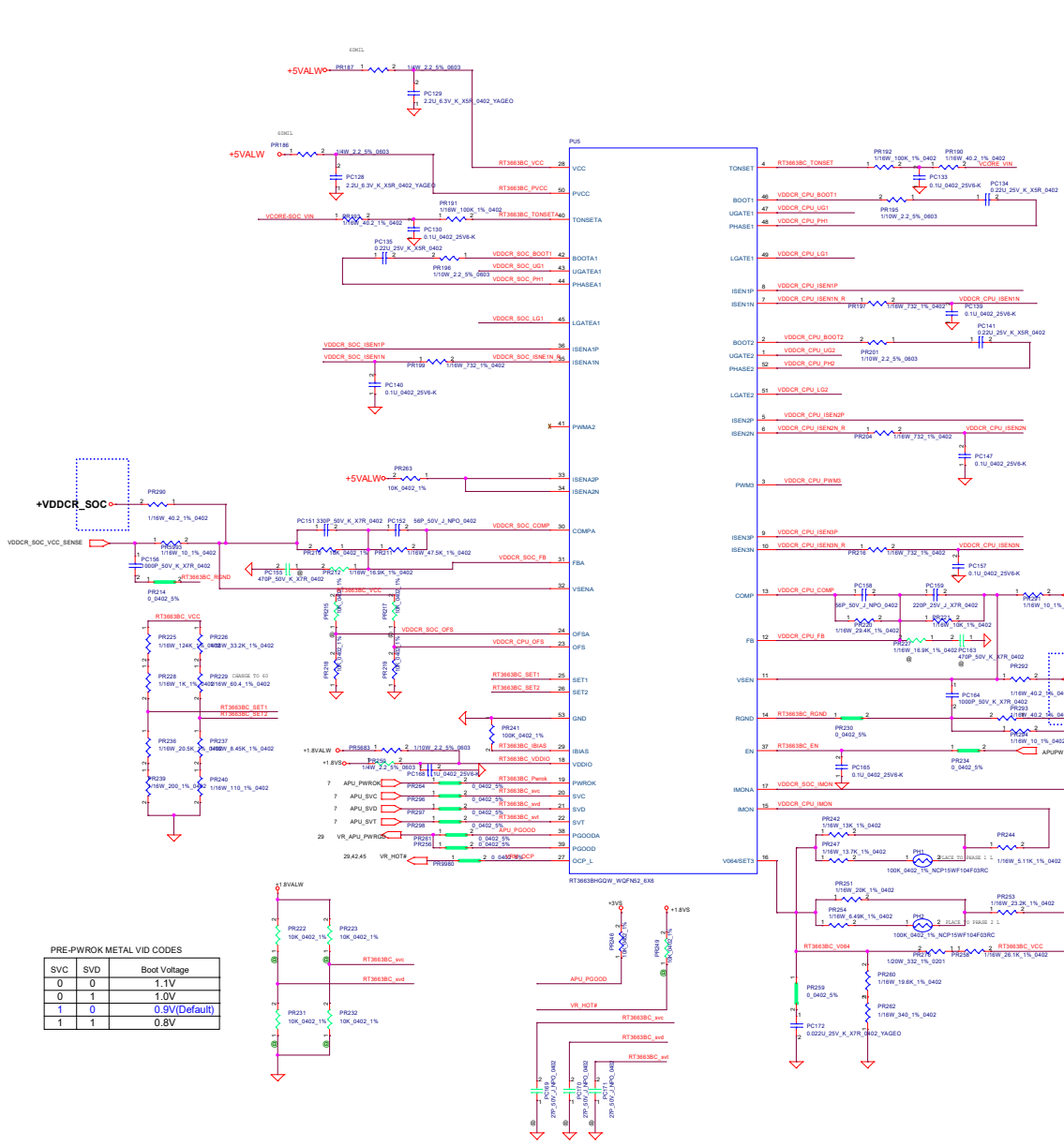


Security Classification		LC Future Center Secret Data		Title	
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2018/03/26		2019/06/01			
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Vset=5.1V±1%
 Design Current:8A
 OCP: Min:9A, Max:11.8A
 OVP=(1.15~1.25)*Vout
 UVP=0.6*Vref
 Fsw=750Khz

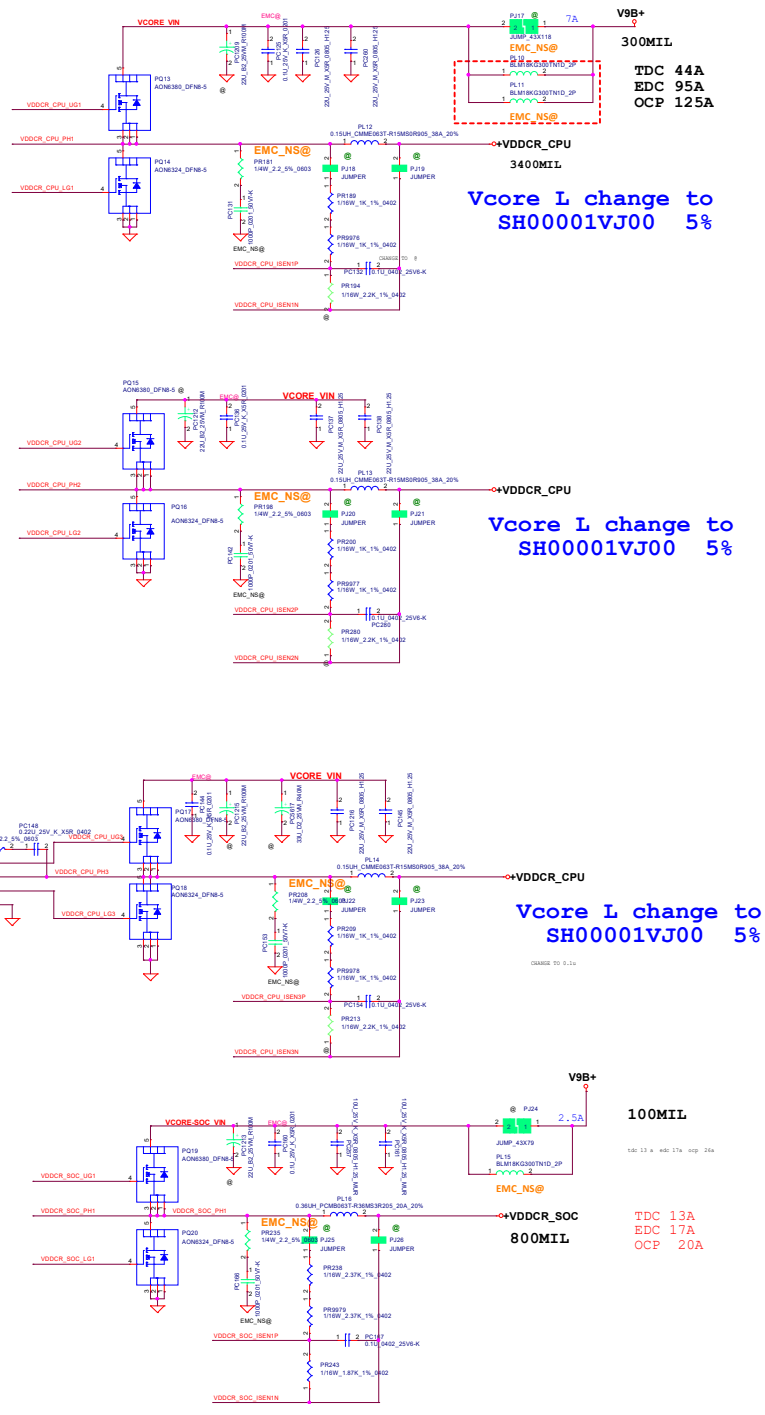




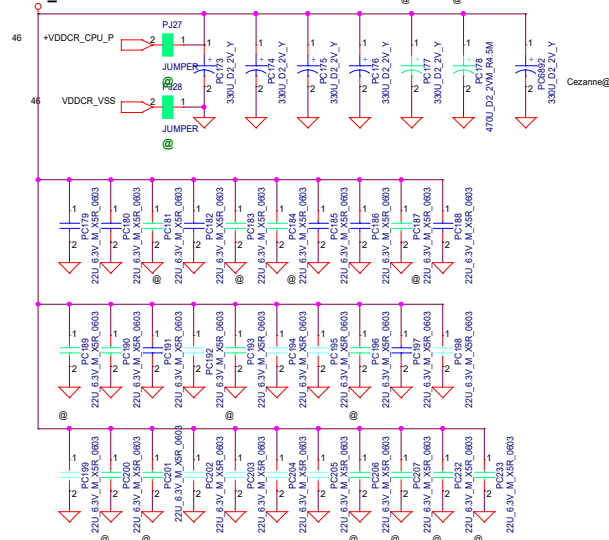
PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

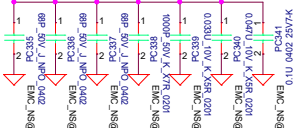
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+VDDCR_CPU

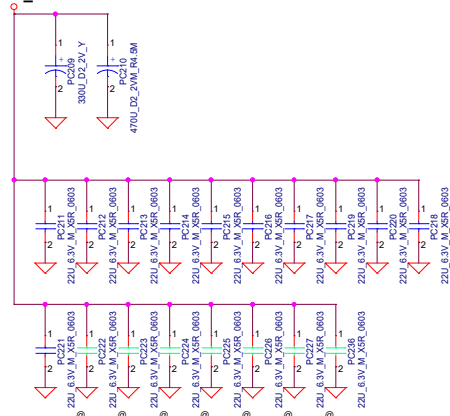


+VDDCR_CPU

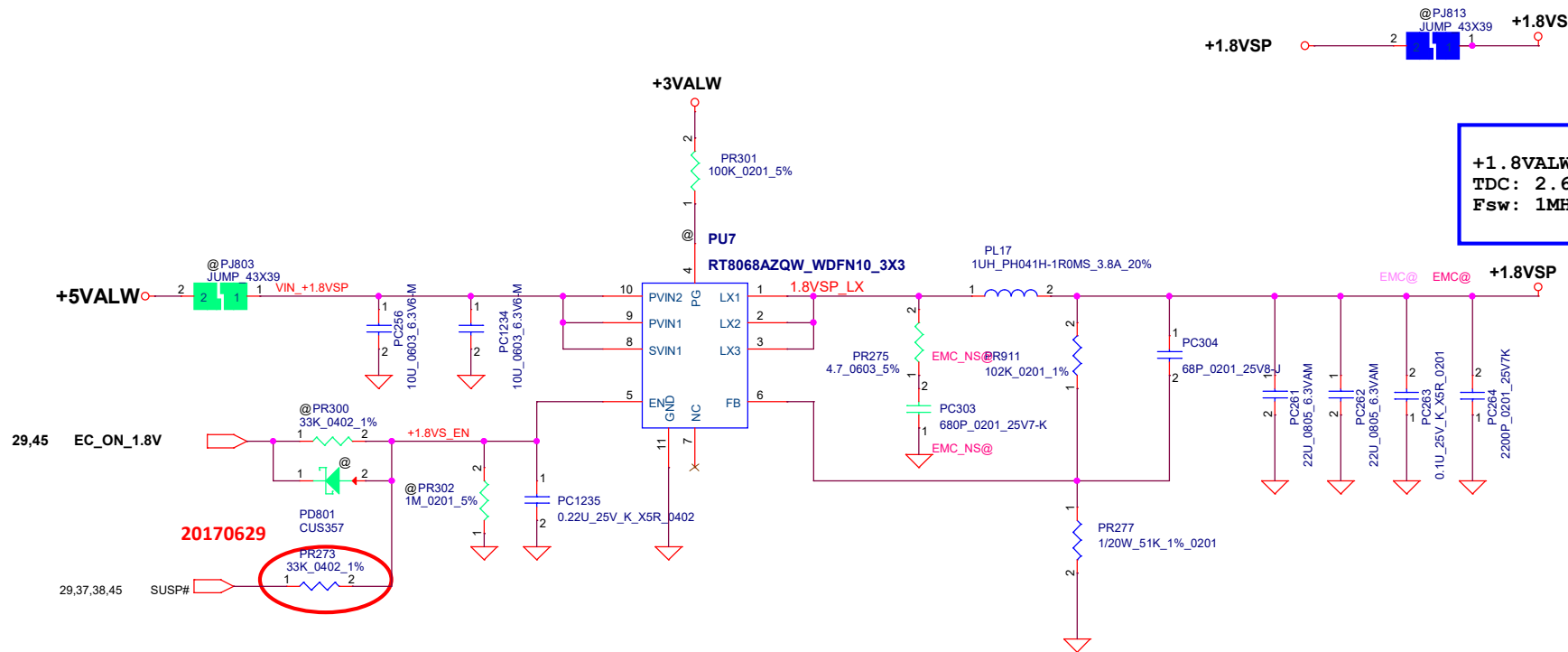



Note
330uF/9mohm*2pcs
22uF/0603*20pcss

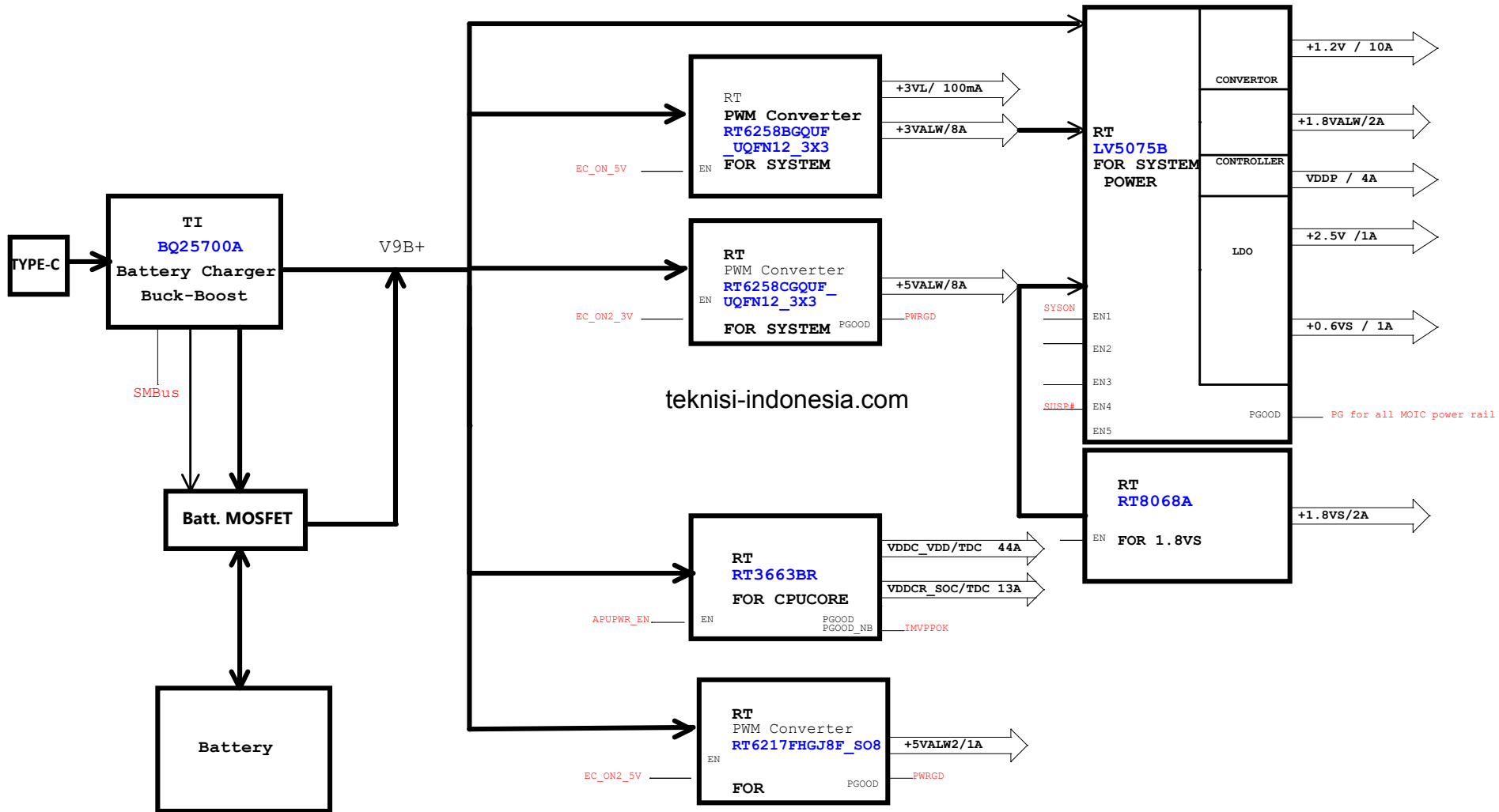
+VDDCR_SOC



330uF/9mohm*2pcs
22uF/0603*16pcss



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1,change 5V back to LV6228CGQUF
 2,add 0.75V and 1.2V remote sense and device sense
 3,change the charger folow T14
 4,change the 1.8V input power to 5Valws
 5,add 5Von off page
 6,add +3V_PWRGD offpage
 7,change 0.75V /1.8Voutput cap0603 to 0805
 8,change Vcore and Vcore SOC input cap to 0805
 9.change the charger output cap to 0805
 10,change the 1.2V output cap
 11,change the input cap 0805 to to 0805 of SE0000QK2D
 12,change netname 5Valw 2 to +5Valws_2


20190702

1,chang the +5VALW2_Mode to the mode pin
 2,change input cap to SE00000QKMT
 3,delete APU power ok pull high of power side

2019.7.8

1,change Vcore highside mofet to AON6380
 2,chaneg 1.2V to AONR32340C
 3,delete some Vcore input cap and output cap follow S540

<Variant Name>

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